Space goes multi-core
Overview of the ESA Next Generation Microprocessor development

GR740 User Day – 13 December 2022

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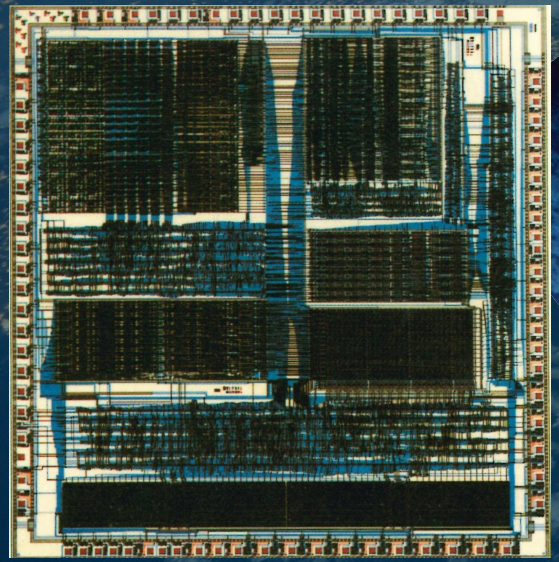
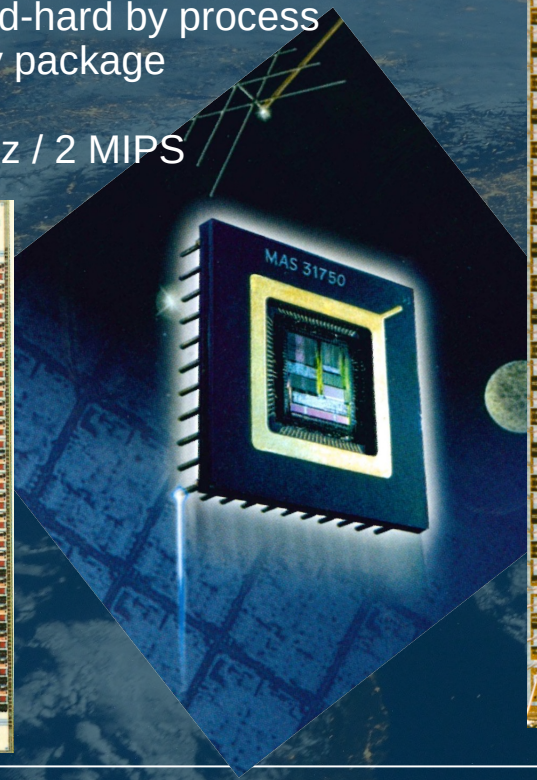
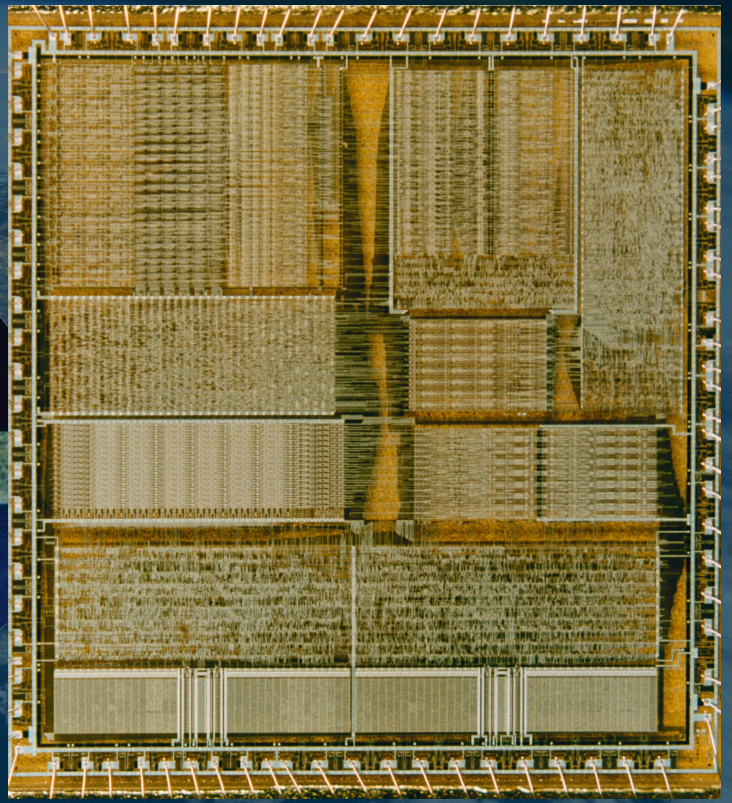
History: Dynex MA31750

First ESA space microprocessor (beg. 90's)
1.25 µm CMOS MEDL/GEC-Plessey/Mitel/Dynex
SOS (Silicon-On-Saphire) = rad-hard by process
84-pin flat-pack / pin-grid array package
16-bit MIL-STD-1750 CISC
2 chip-set (CPU/MMU), 16 MHz / 2 MIPS







History: ERC32 chipset: first 32-bit SPARC V7

First ESA SPARC microprocessor (1991 - 1997, obsolete 2002)

- **32**-bit **E**mbedded **R**eal-time **C**omputing core
- Commercial IP-core, basic SEU protection: parity on all registers
- 0.8 µm CMOS Temic/Atmel fab (now Microchip)
- Used on DMS-R (Zvezda module of ISS)
- 256-pin quad-flat-pack (MQFP) package
- 3 chip-set (CPU/FPU/MEC)
- 32-bit SPARC-V7 RISC
- 14 MHz / 10 MIPS

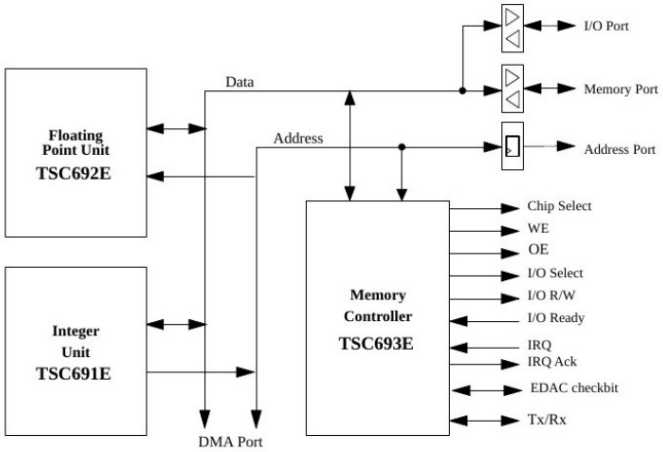
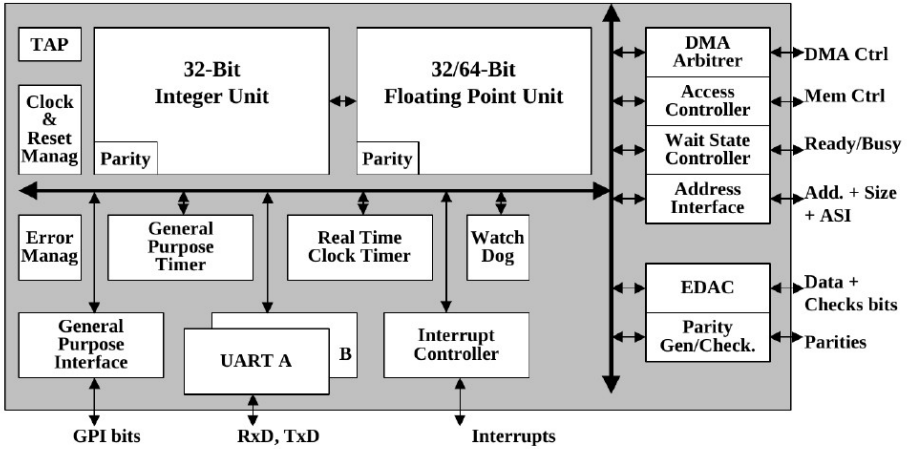


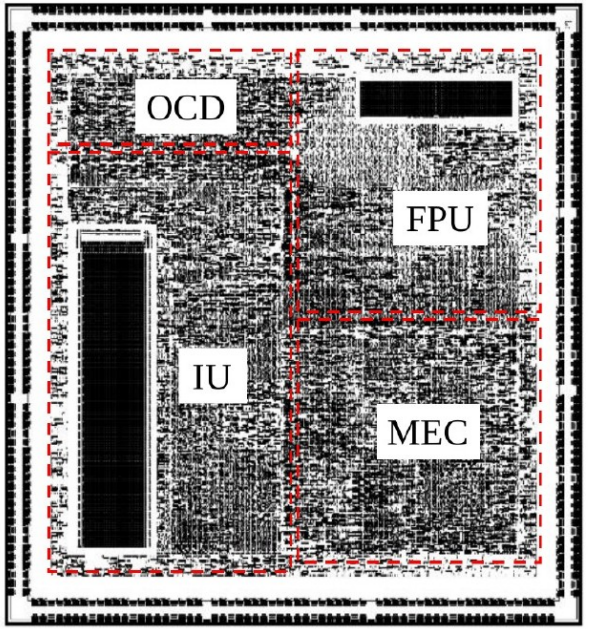
Figure 1. ERC32 Architecture

History: ERC32 Single Chip

Second generation ESA SPARC microprocessor (end 90's, still on Microchip catalog)

- 0.5 µm CMOS Temic/Atmel fab (now Microchip)
- Shrink: same design and IP as ERC32 chip-set, but now in one chip
- Extended SEU protection, parity + hardened flip-flops (HDFF)
- Widely used across many ESA projects Ariane 5 IMU, GOCE, AEOLUS, CRYOSAT...
- 256-pin quad-flat-pack (MQFP) package
- 32-bit SPARC-V7 RISC
- 25 MHz / 20 MIPS

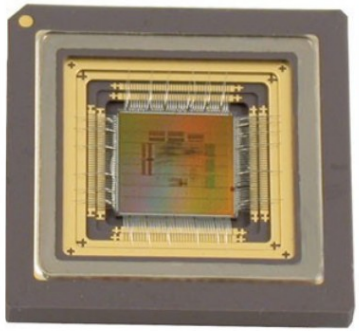


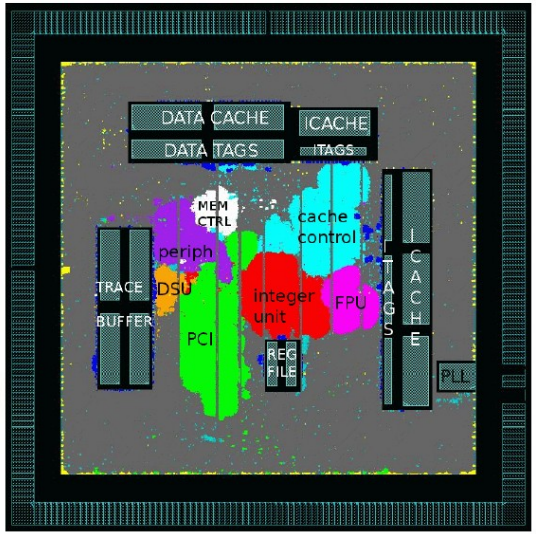


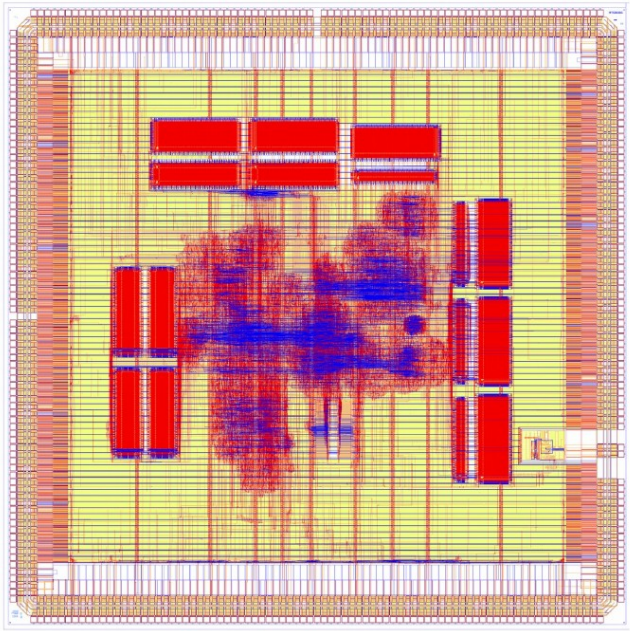
History: AT697 – first LEON

First generation ESA LEON-SPARC microprocessor (on Microchip catalog)

- 0.18 µm CMOS Temic/Atmel fab, later ported to UMC fab
- Based on ESA LEON2-FT IP core, SRAM/SDRAM port, PCI 2.3 interface
- SEU protection: cache parity, reg-file EDAC, TMR flip-flops + skewed clocks, *no HDFF*
- First launches: Airbus Ernobox on ISS (March 2008), PROBA-2 OBC (Nov. 2009)
- MCGA/LGA 349 and 256-pin MQFP package
- 32-bit SPARC-V8 RISC, 100 MHz / 86 (D)MIPS



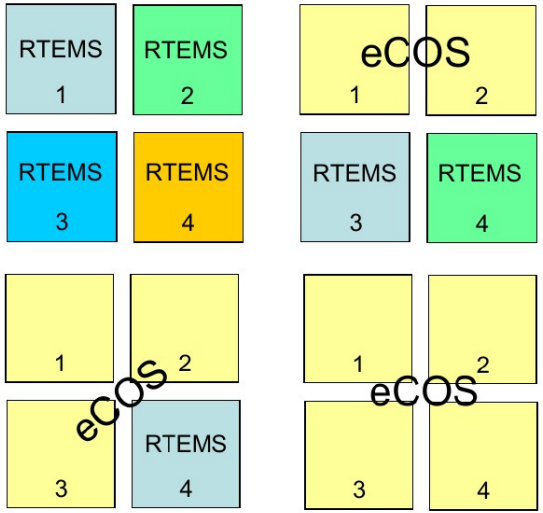




NGMP Phase 0 – GINA : Space goes multi-core

Phase 0: GINA (Giga-Instruction New Architecture)

- 2006, multi-core study, LEON3-FT quad-core system, FPGA demonstrator (Virtex4-LX200)
- 2-bus system (CPU/peripheral bus) – bottleneck in the 32-bit CPU bus
- Virtex4, high utilisation, FPGA tool issues: 40 MHz (4-cores) / 80 MHz (1-core)
- Estimate: 266 MHz (90 nm techn)
- ASMP operation: 4 x RTEMS
- SMP operation: eCOS only
- Mixed mode configurations



4 cores on 32-bit AHB = **bottleneck**

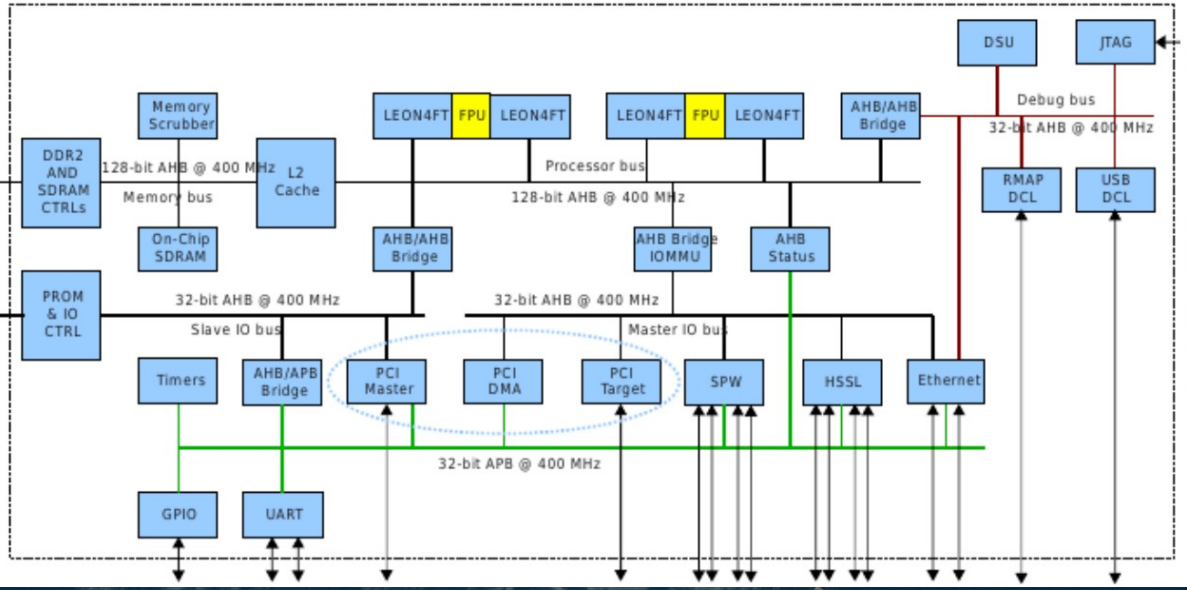
Phase 1: N2X prototypes

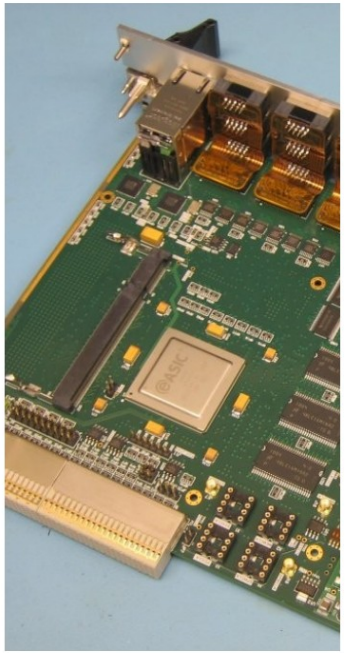
Phase 1: Definition and Architectural Design of Multi-core SPARC NGMP

- Competitive ITT in 2008 won by (Aeroflex) Gaisler, contract signed 2009
- Mandatory use of ST 65 nm space platform (under ESA development), LEON not mandatory
- Spec published in 2010: LEON4, L2-Cache, 128-bit CPU bus, DDR2, Serdes, debug and 2 I/O busses
- FPGA demonstrator boards released to users in 2010

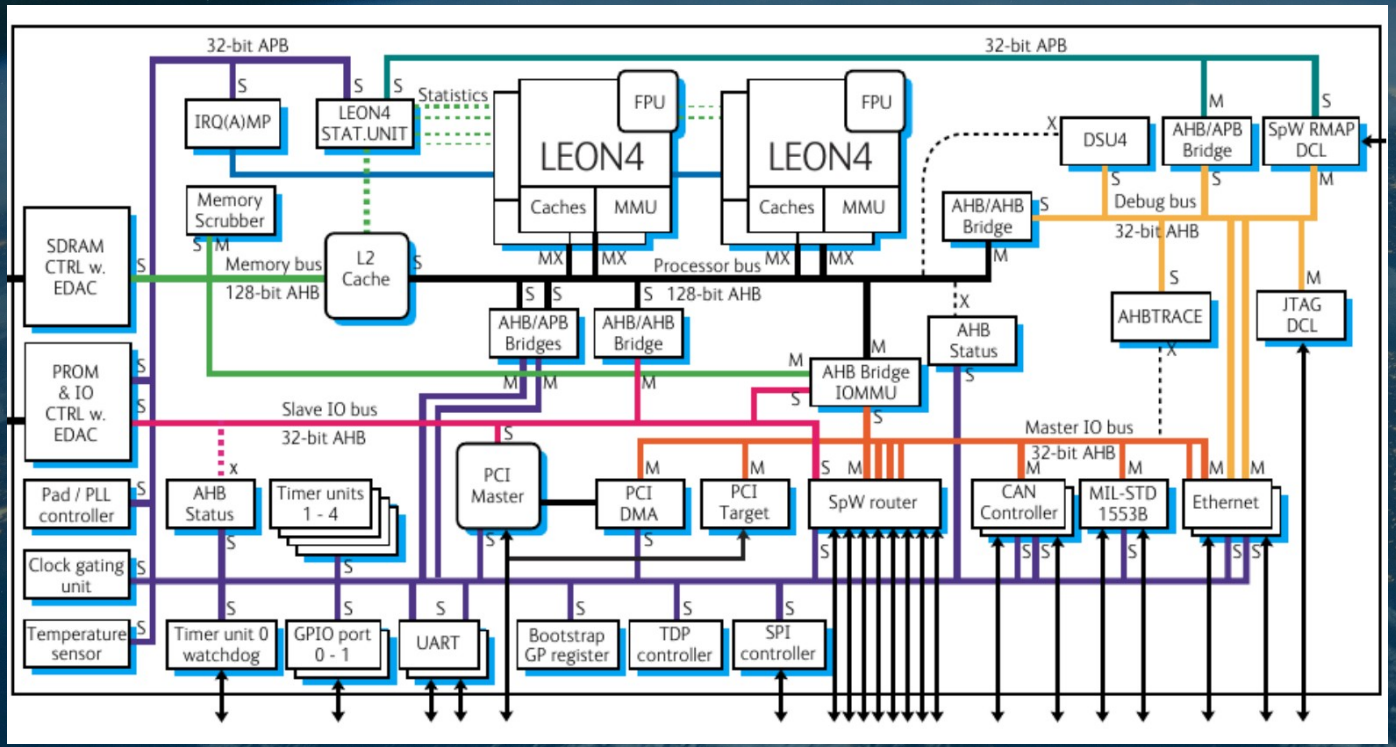
On-hold for 3 years (waiting for ST 65nm readiness and access)

- LEON4-N2X: prototypes in commercial eASIC in 2013





Waiting for technology : design improvements

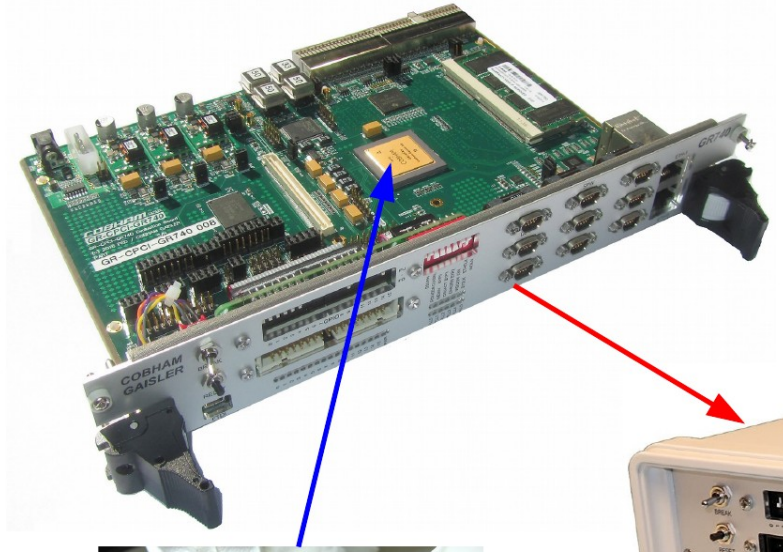


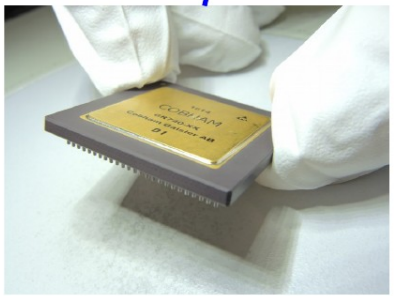
- Spacewire router
- CAN Controller
- MIL-1553, SPI
- Statistics unit

- Multicore ¨fixes¨ to improve predictability
  - AHB split
  - L2 locking
  - Cache random replacement

- Technology limitation
  - ~~DDR interface~~
  - ~~SerDes~~

Phase 2: GR740 Prototypes

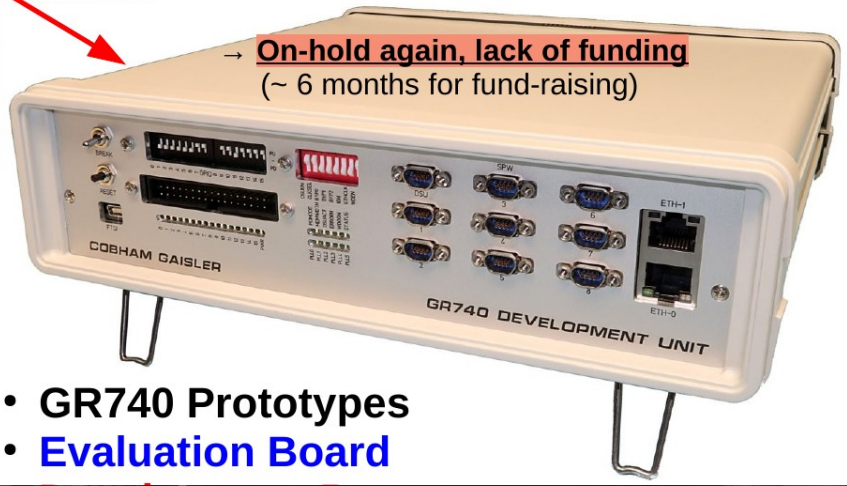




Phase 2: GR740 Prototypes (resumed 2014)

- Added split-support to L2-cache, SPW router
- DDR2 SDRAM removed (no IO's / PHY)
- Flip-chip was high risk, use wire-bond instead
- → SERDES removed (IP for flip-chip only)
- Sign-off, ready for ST fab: June 2015
- First Prototypes delivered by ST in Jan. 2016
- Functional validation + radiation testing
- Evaluation board released (June 2016)
- EM and boards out of stock in autumn 2016

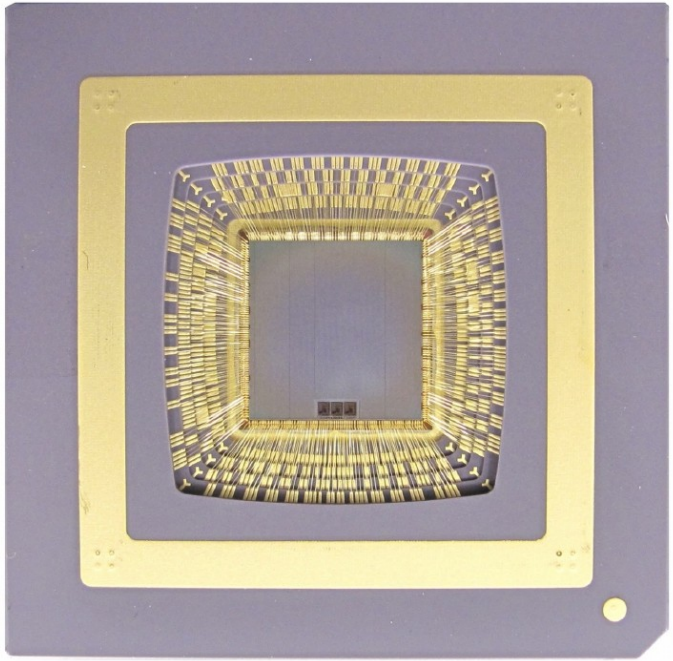
→ **On-hold again, lack of funding**
(~ 6 months for fund-raising)

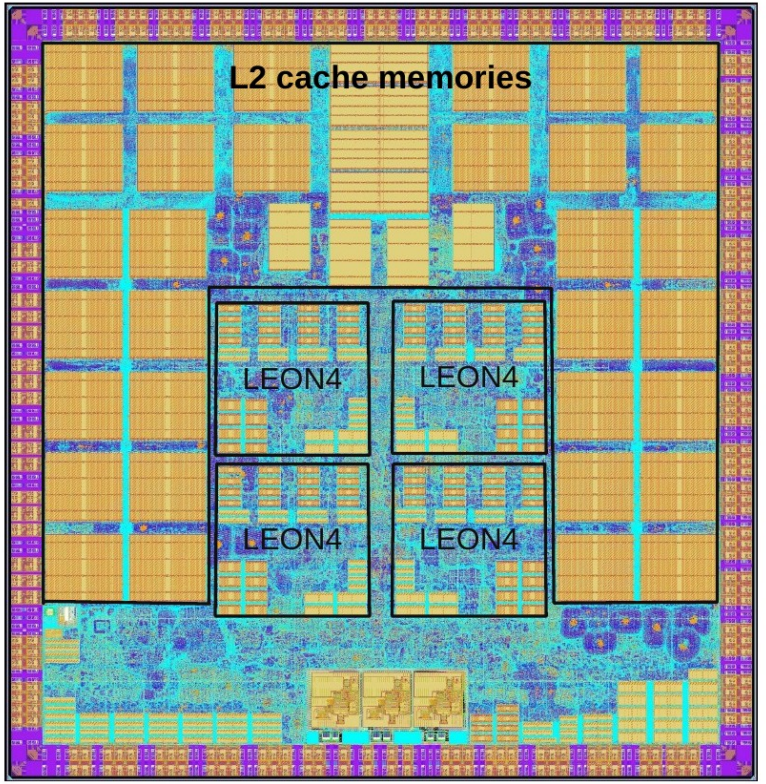


- **GR740 Prototypes**
- **Evaluation Board**

Phase 3: GR740 Flight Parts

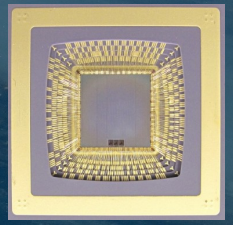
- Design updates and fixes (2017)
- Flight silicon manufactured (Q1/2018)
- Functional validation + radiation testing
- Packaging challenge (OPM, wire-bonding)
- **Flight parts Q4/2021, QML-V Q2/2022**





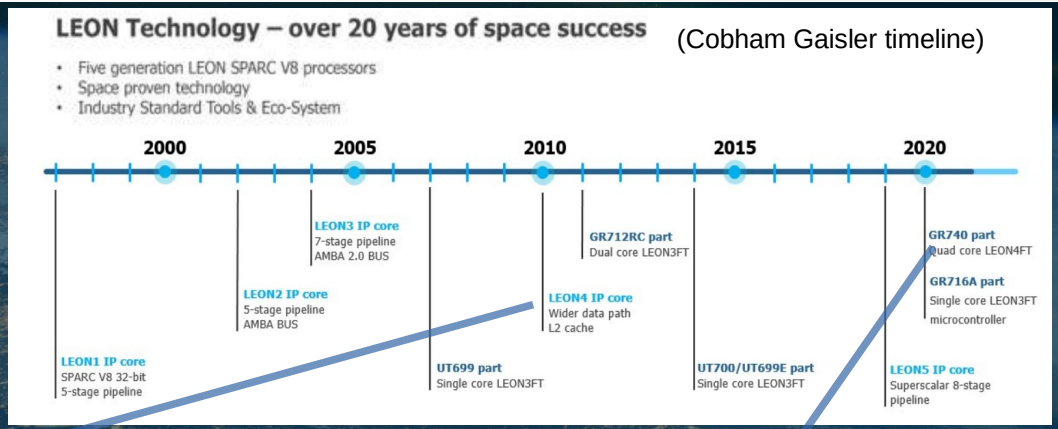
Funding? – Making chips on a shoestring

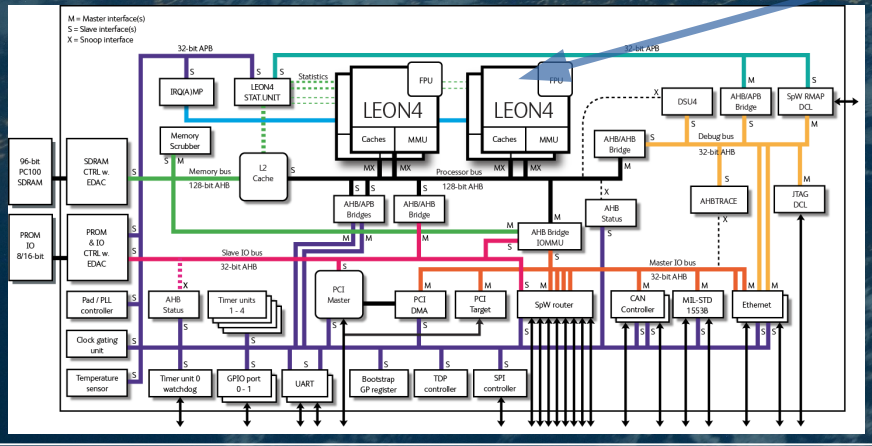
- NGMP / GR740 chip development: ~ 3.8 M€ ESA + 1.2 M€ co-funding
  - Design is based to a large extent on background IP (= additional co-funding)
- > 2 M€ ESA funding on accompanying SW activities
  - RTEMS-SMP and Qualification
  - Benchmarking and predictability studies
  - Hypervisor developments
  - Compiler, BSP, boot SW : significant company investment
- Expenditure spread over ~2009 – 2021 (~ ½ M€ / year) → several hold periods ...
  - Technology unavailability : 65 nm platform & packaging technology
  - Waiting for budget : ¨funding comes in droplets¨



2022: qualified chip, software and … users

- GR740 quad-core LEON4FT
  - 65 nm ST-Microelectronics
  - FM in Q4/2021
  - QML-V in Q2/2022
  - Plastic variant (ARTES)
- Comprehensive SW ecosystem
- Many users in North-America, Europe, Middle-East and Asia
- **First launch in Dec 2022**





Welcome to ESTEC

for the 2022 edition of the

GR740 User Day