Reference Design and Basic Software for a Single Board Computer based on GR740

Reference design activity and future plans

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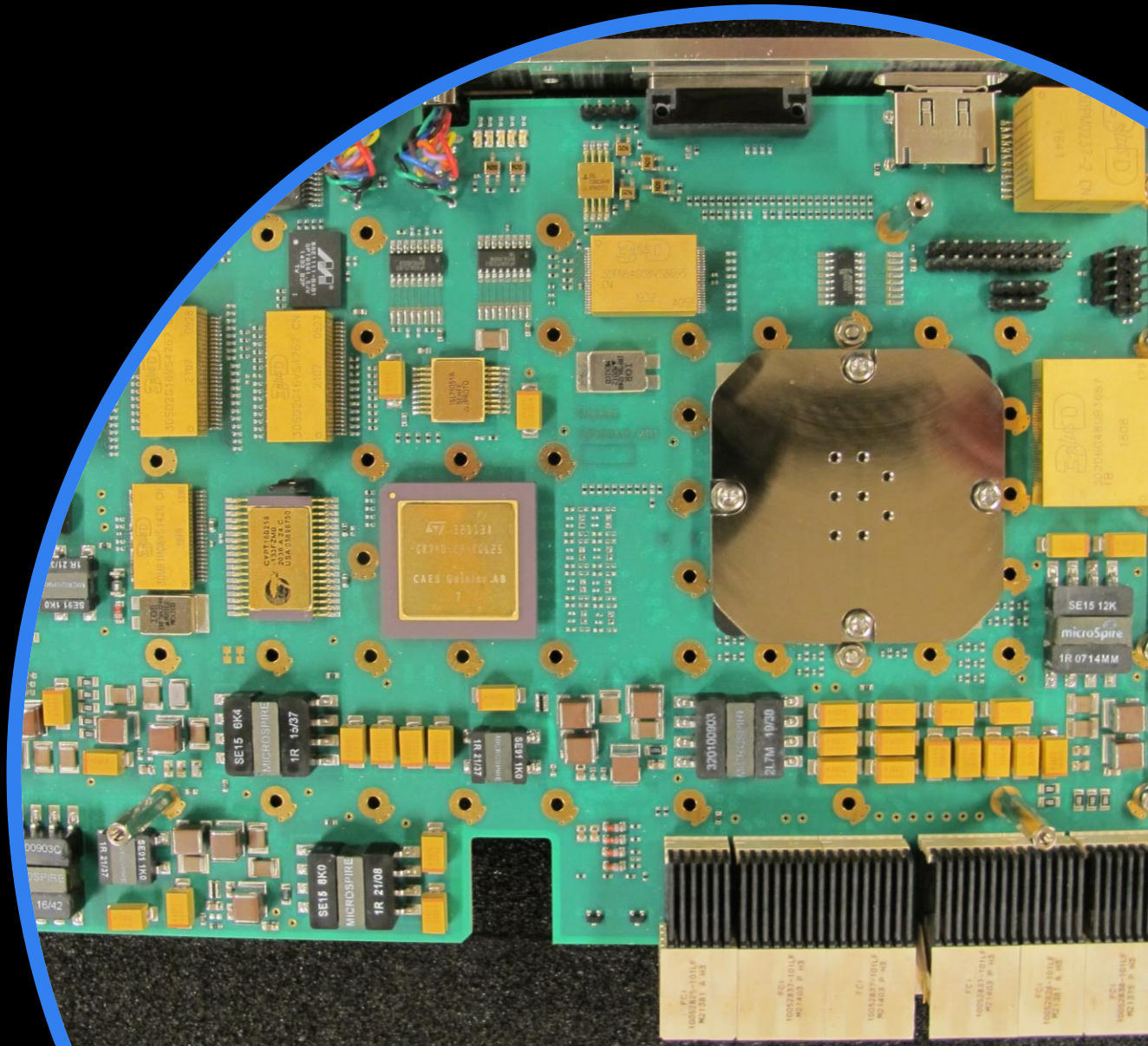
GR740 SBC Development Introduction



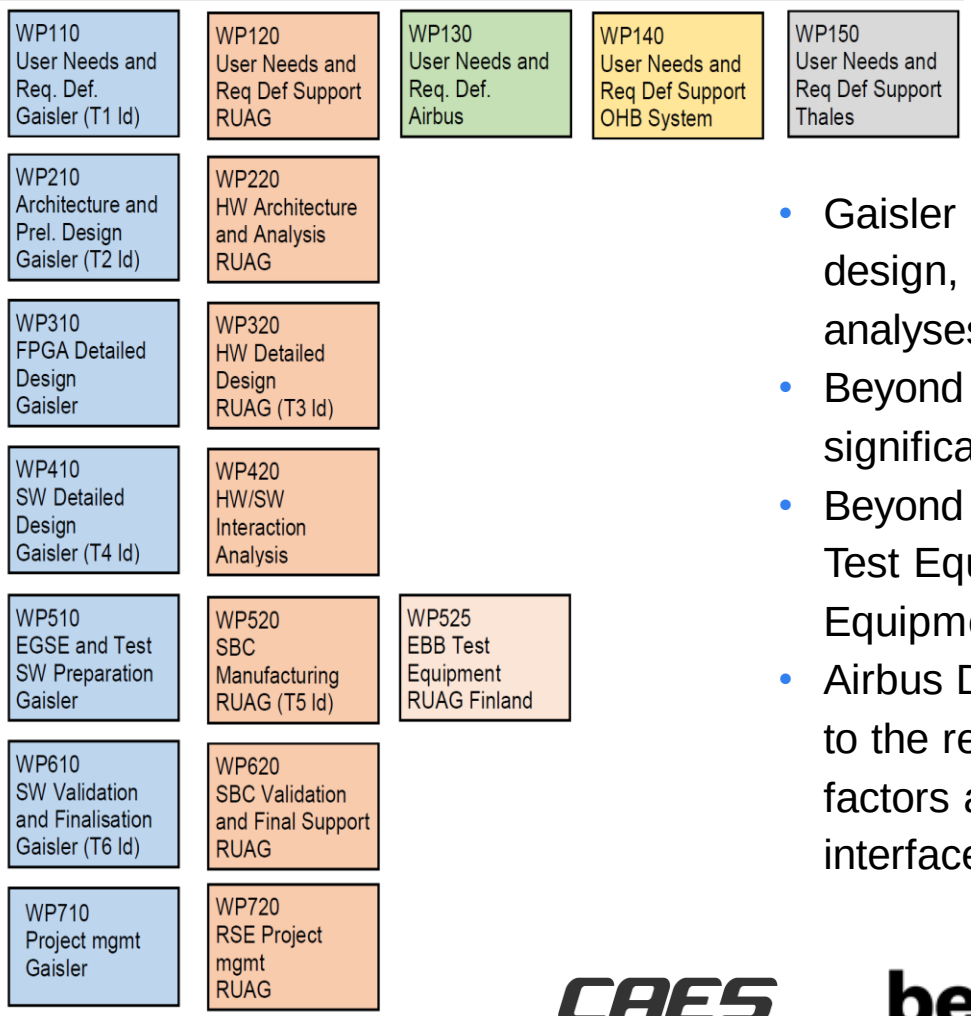
GR740 SBC activity

- ESA activity “Reference Design and Basic Software for a Single Board Computer based on GR740”

- Main objectives
  - To create a single board computer reference design using the GR740, available to all European space users.

  - Reference design data package
  - Development of Elegant Breadboard
  - Verified at functional and performance level (TRL 4)
  - Supported by a Qualification Test Plan
  - Supported by boot software, device drivers and test application software

Overview of the GR740 SBC activity



- Gaisler - responsible for the overall activity, the software design and the FPGA design, as well as contributing to the system architecture and hardware design and analyses; project management of the entire consortium.
- Beyond Gravity Sweden - responsible for the hardware design and validation, and for significant parts of the hardware analyses.
- Beyond Gravity Finland - responsible for defining and specifying the in-house EBB Test Equipment and to define test cases and supervise the manufacturing of the Test Equipment.
- Airbus Defence and Space, OHB System and Thales Alenia Space - input provided to the requirements and the architecture of the GR740 SBC: general features, form factors and hardware and software aspects; support to the overall plans focusing on interfaces and risk assessments, and participation in the SRR.

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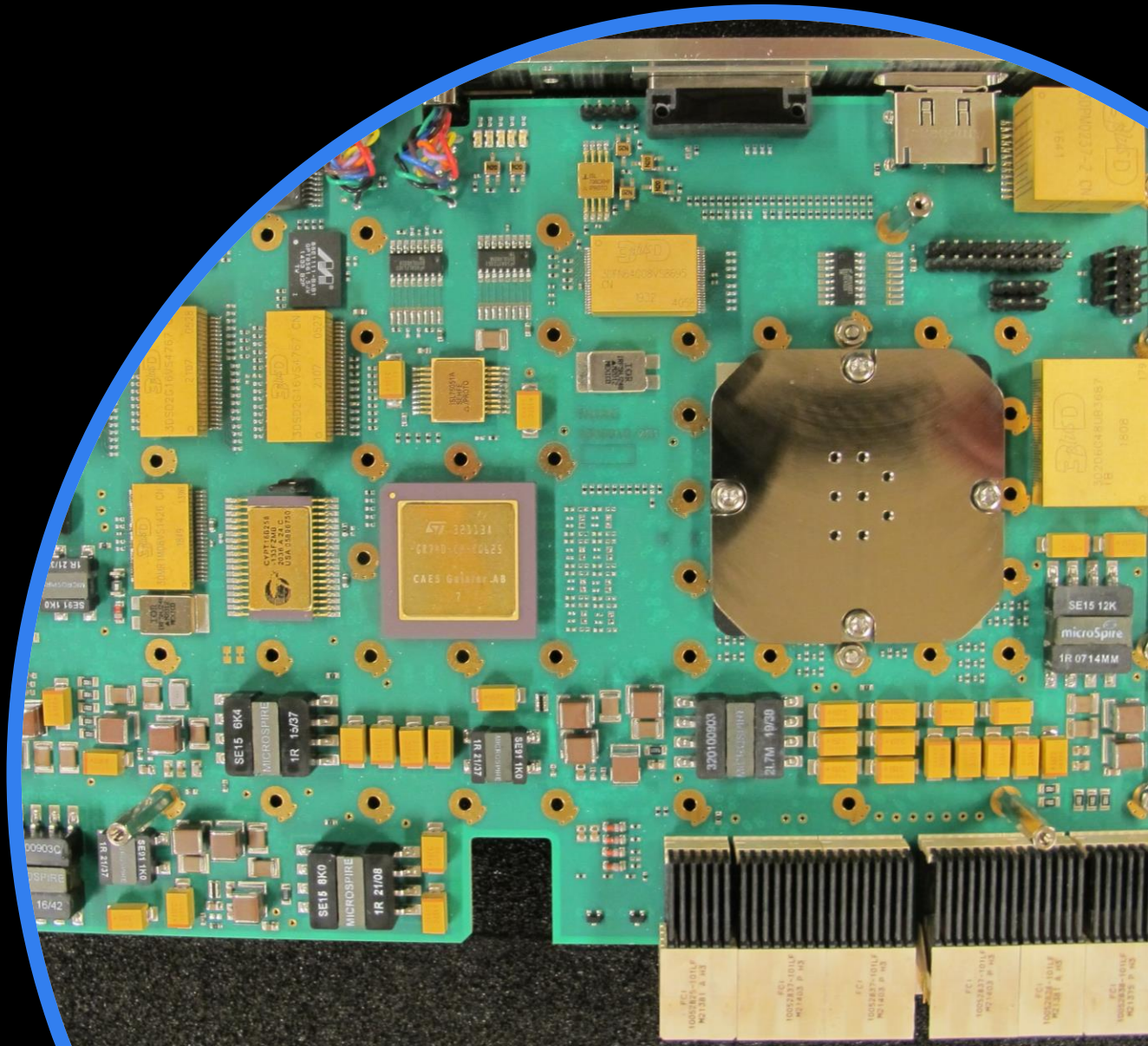
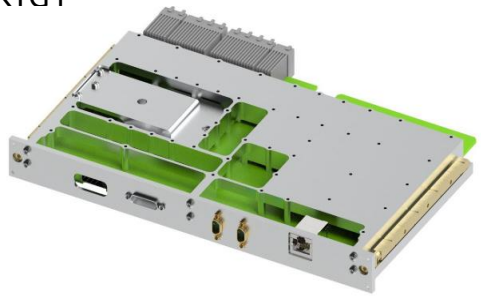
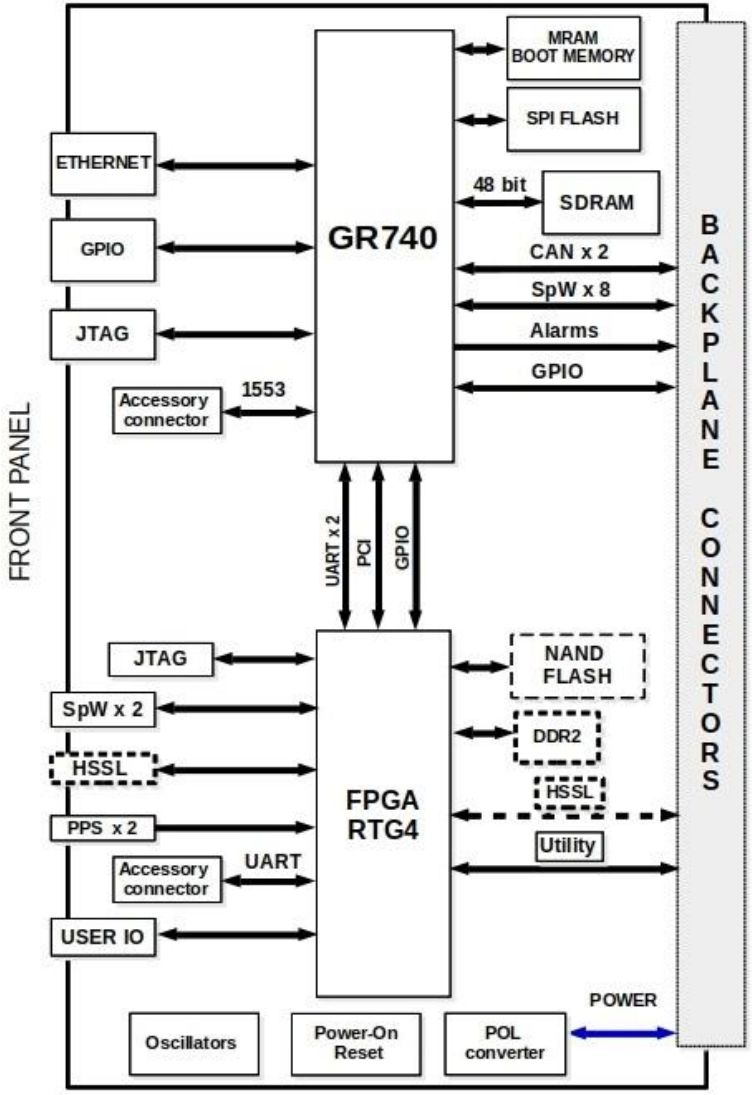
Hardware Overview



GR740 Single Board Computer - Overview

- A high-performance Single-Board Computer based on GR740 quad-core 32-bit LEON4FT SPARC V8 processor and Microsemi RTG4 radiation tolerant FPGA.
- The SBC provides an extensive set of memories and redundant interfaces to support the needs of current and future OBC and Data Handling platforms.
- Features
  - Implemented following the Compact PCI Serial Space backplane standard (CPCI-S.1 R1.0)
    - Dual star, eight SpaceWire interfaces from GR740
    - Multi drop bus, redundant CAN from GR740
    - Full mesh, HSSL (SpFI) from RTG4
    - Multi drop bus, I2C from RTG4
    - Alarms and other utility signals
  - On-board memory
    - SDRAM interfaced with GR740, 512 MIB of accessible data RAM plus ECC check bits
    - Parallel Boot MRAM, 64 KiB interfaced with GR740
    - SPI Flash memory, 32 MiB interfaced with GR740
    - 3D-PLUS NAND FLASH, 8 GiB interfaced with RTG4
    - 3D-PLUS DDR2, 512 MiB of accessible data RAM plus ECC check bits interfaced with RTG4
  - PCI, UART and GPIO interface between GR740 and RTG4
  - Interfaces at front edge of board:
    - 2 x SpaceWire
    - Gigabit Ethernet
    - General purpose I/O's
    - PPS (Pulse Per Second) input for synchronization (SMB)
  - Form factor
    - 6U (233.5 mm x 160 mm), 5 HP. Mass 1.2 kg (estimate)
  - Power consumption: ~30 W (worst case estimate, also assuming 100 % FPGA utilized)
- SBC included with DDR2, NAND FLASH and HSSL as extensions





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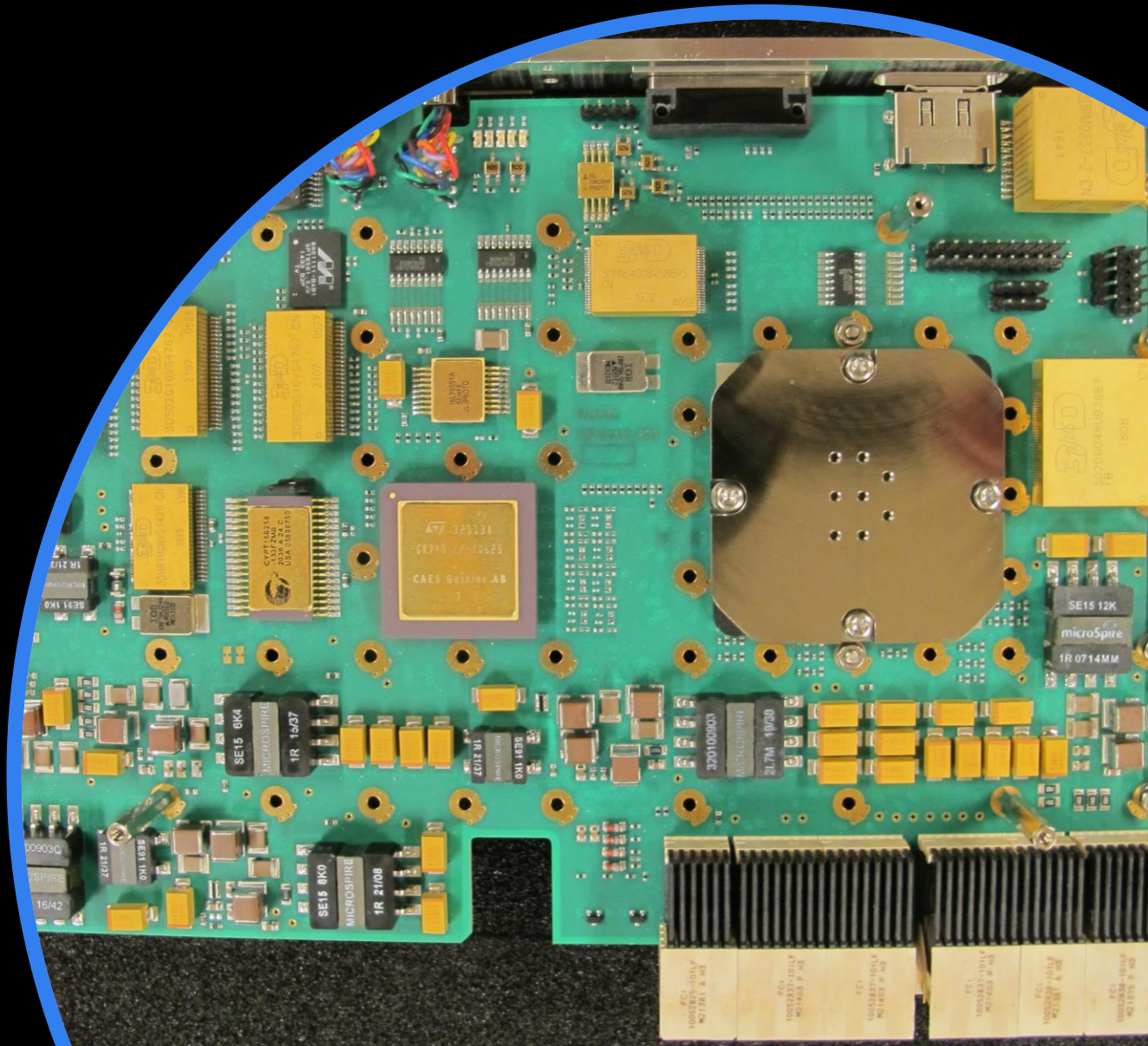
Software & FPGA Description



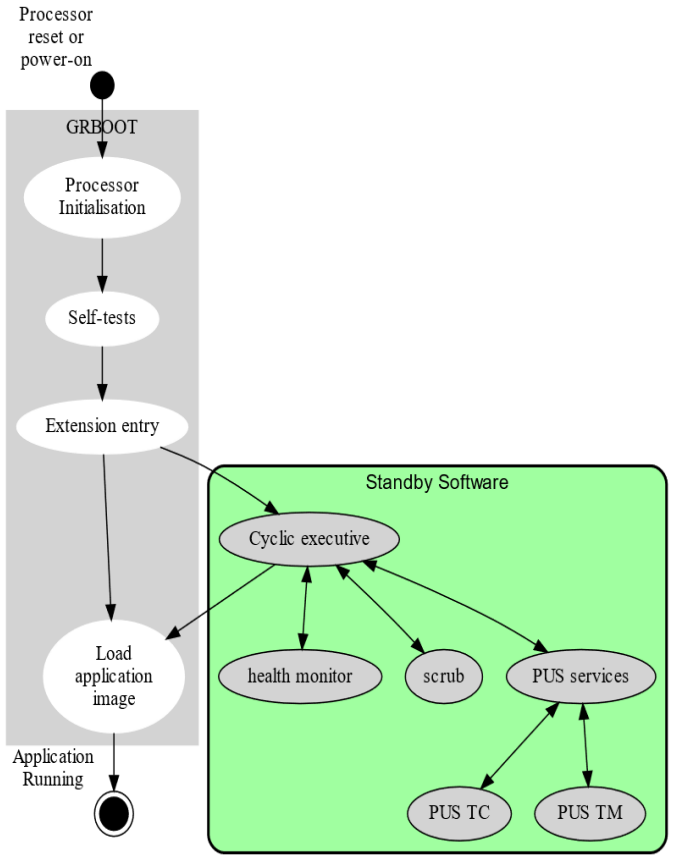
SBC software description

- The SBC is supported by boot software, device drivers and test application software

- Boot Software
  - The Boot Software is responsible for taking the GR740 from system reset state to the execution of multi-processor mission application software

- Peripheral drivers for:
  - GR740 CAN controller
  - GR740 PCI host controller
  - GR740 SPI controller
  - These drivers will complement the software environment output from ESA activity "Qualification of RTEMS-SMP" to create better RTEMS-5 SMP support for the GR740 SBC

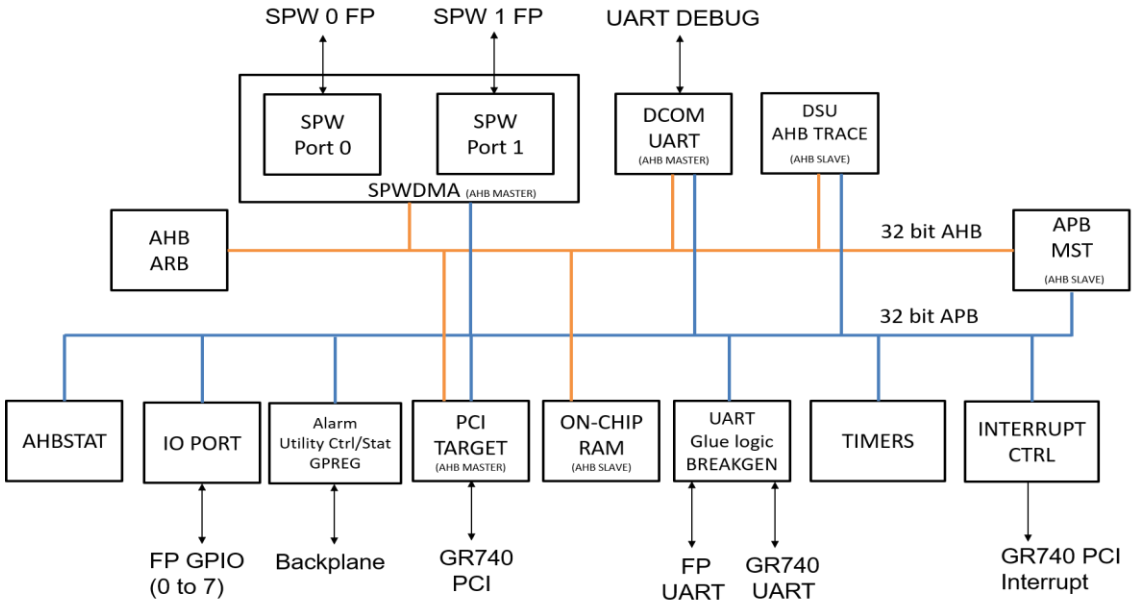
- Test application
  - The focus for the Test Application (TA) and EGSE SW is to verify the board interfaces and memories on a functional level
  - The TA and EGSE SW developed in this activity can be reused and extended for a specific implementation of the GR740 SBC platform simplifying an efficient functional verification of the hardware platform



FPGA VHDL design

- FPGA design with source code part of the reference design data package.
- Most IPs are from the ESA LEON2FT package.

- FPGA VHDL design
  - Interface for communication with GR740, PCI target implementation
  - AMBA 2.0 bus fabric for integration of different IP's with AMBA support
  - On chip memory
  - UART Glue logic, to provide additional features to support the SAVOUIR UART spec
  - General purpose IO ports
  - Status, interrupt interface between FPGA and the GR740
  - Utility and Alarm signal handling
  - PPS distribution



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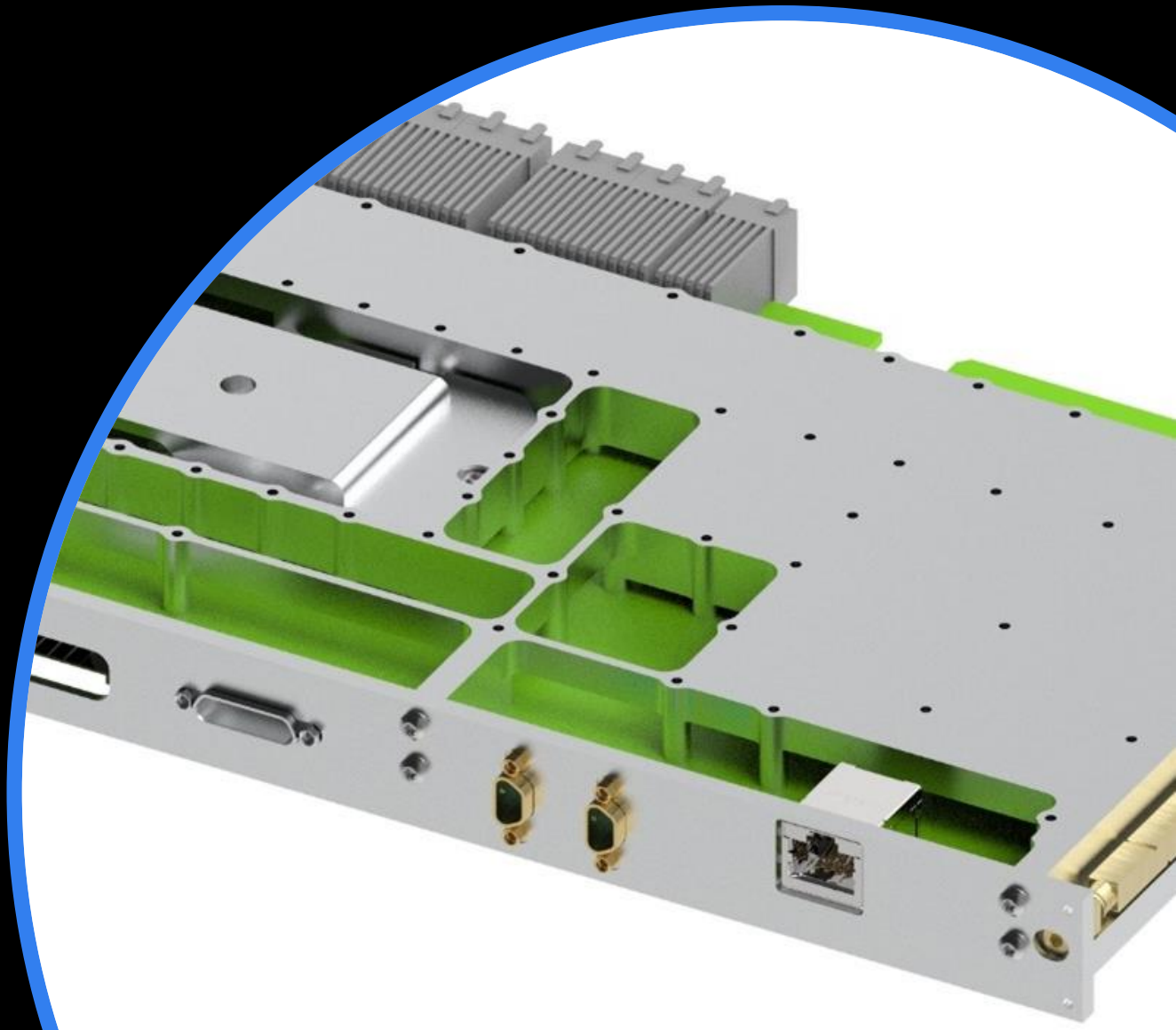
Hardware Design Description



Compact PCI Serial Space

- A trade-off has been performed comparing the two backplane standards:
  - SpaceVPX (ANSI/VITA 78-2015)
  - Compact PCI Serial Space (CPCI-S.1)

- The **GR740 SBC implements the Compact PCI Serial Space** backplane standard
  - The form factor of the board is 6U (233.5 mm x 160 mm)
  - Slot width of 5 HP and an estimated mass of 1.2 kg

- Compact PCI Serial Space has been selected as baseline for ADHA standardization activities, which has support from the European space industry.

- Latest ADHA specifications includes several improvements compared to the cPCIss standard.

Processing capability

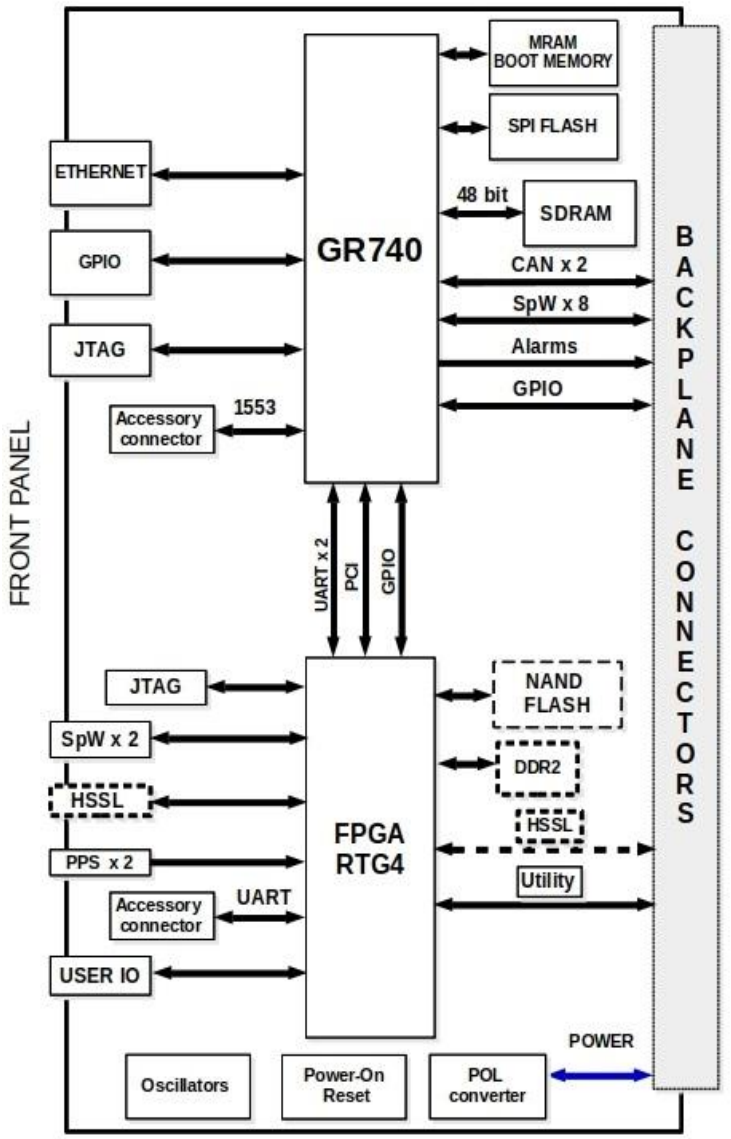
- A high-performance Single-Board Computer based on GR740 quad-core 32-bit LEON4FT SPARC V8 processor and Microchip RTG4 radiation tolerant FPGA.

- GR740 radiation-hard system-on-chip
  - Run at 250 MHz
  - Fault-tolerant quad-processor SPARC V8 integer unit with 7-stage pipeline
  - 4x4 KiB instruction, 4x4 KiB data caches, 2 MiB Level-2 cache
  - Double-precision IEEE-754 floating point units

- Microchip RTG4 radiation tolerant FPGA
  - To implement glue logic and additional required interfaces
  - Application specific developments and implementation of accelerator functions
  - The RTG4 implements the high-speed serial link (HSSL) capability to the SBC
  - The glue-logic required to be compatible with the CPCI-S.1 R1.0 standard are also implemented in the FPGA
  - More than 70 % of the FPGA resources are available for user defined functions

Interfaces between GR740 and RTG4

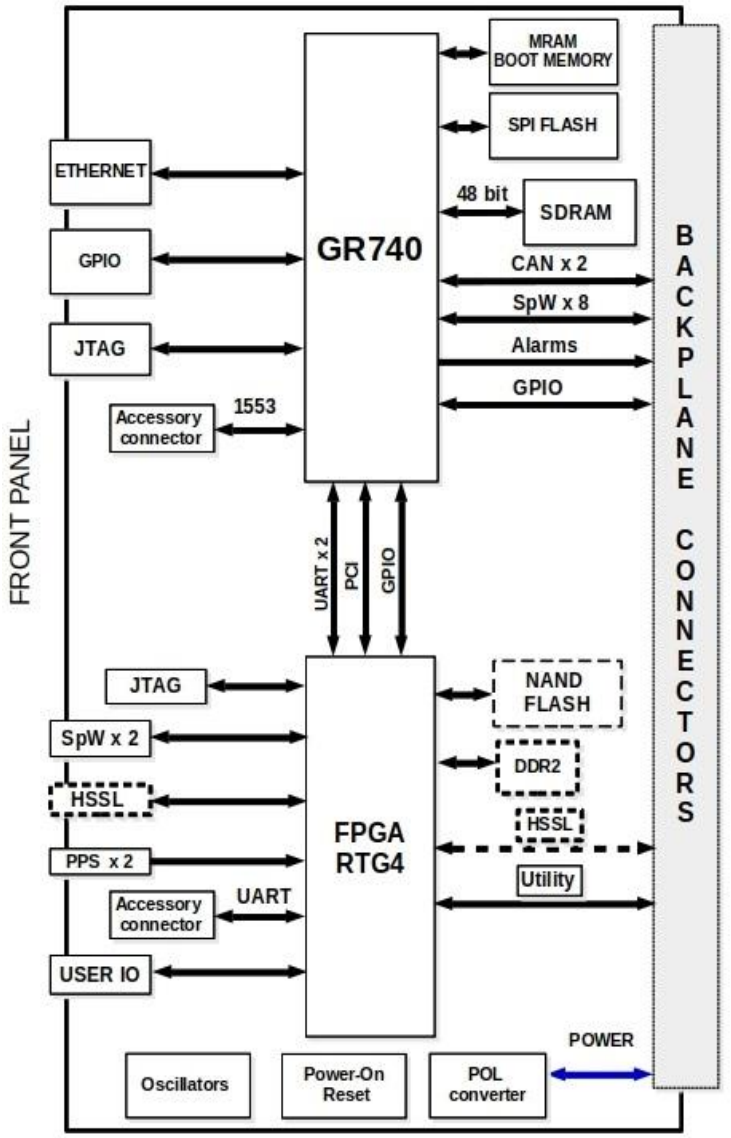
- PCI has been chosen since it provides following advantages compared to other interfaces:
  - PCI memory mapped solution can offer register access with less software overhead compared to using SpaceWire RMAP
  - PCI also provides streaming of data using dedicated DMA available in the GR740
  - Well known and established bus with VHDL IP cores available for FPGA implementation



On-board Memory

- GR740 memories
  - Parallel Boot MRAM, 64 KiB
  - Application storage
    - SPI Flash memory, 32 MiB
  - SDRAM is used for the main processing memory.
    - 512 MIB of accessible data RAM plus ECC check bits
    - The PCI interface on GR740 is pin shared with SDRAM memory interface.
    - Since PCI is used to interface with FPGA only half 48 bits of the available 96 SDRAM data bits are used for memory interface

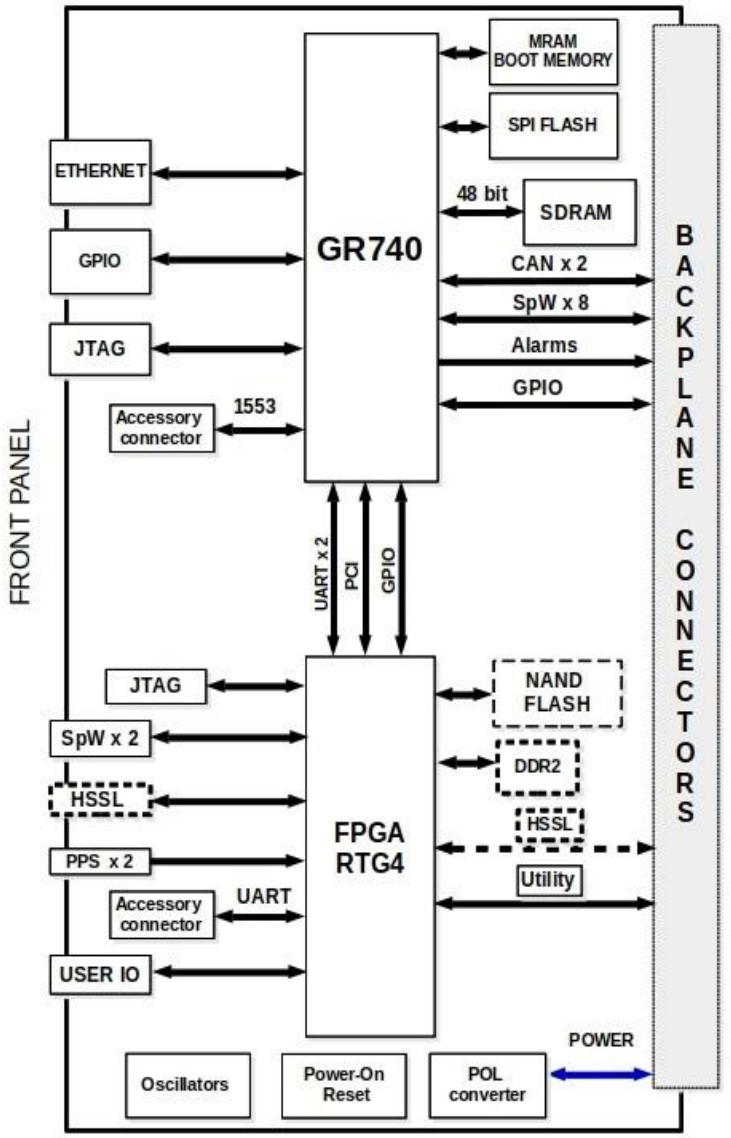
- RTG4 memories
  - Platform Data Storage for non-volatile storage of data
    - 3D-PLUS NAND FLASH, 8 GiB interfaced with RTG4
  - Additional volatile memory for the user defined FPGA based functions
    - 3D-PLUS DDR2, 512 MiB data RAM plus ECC check bits interfaced with RTG4



Interfaces

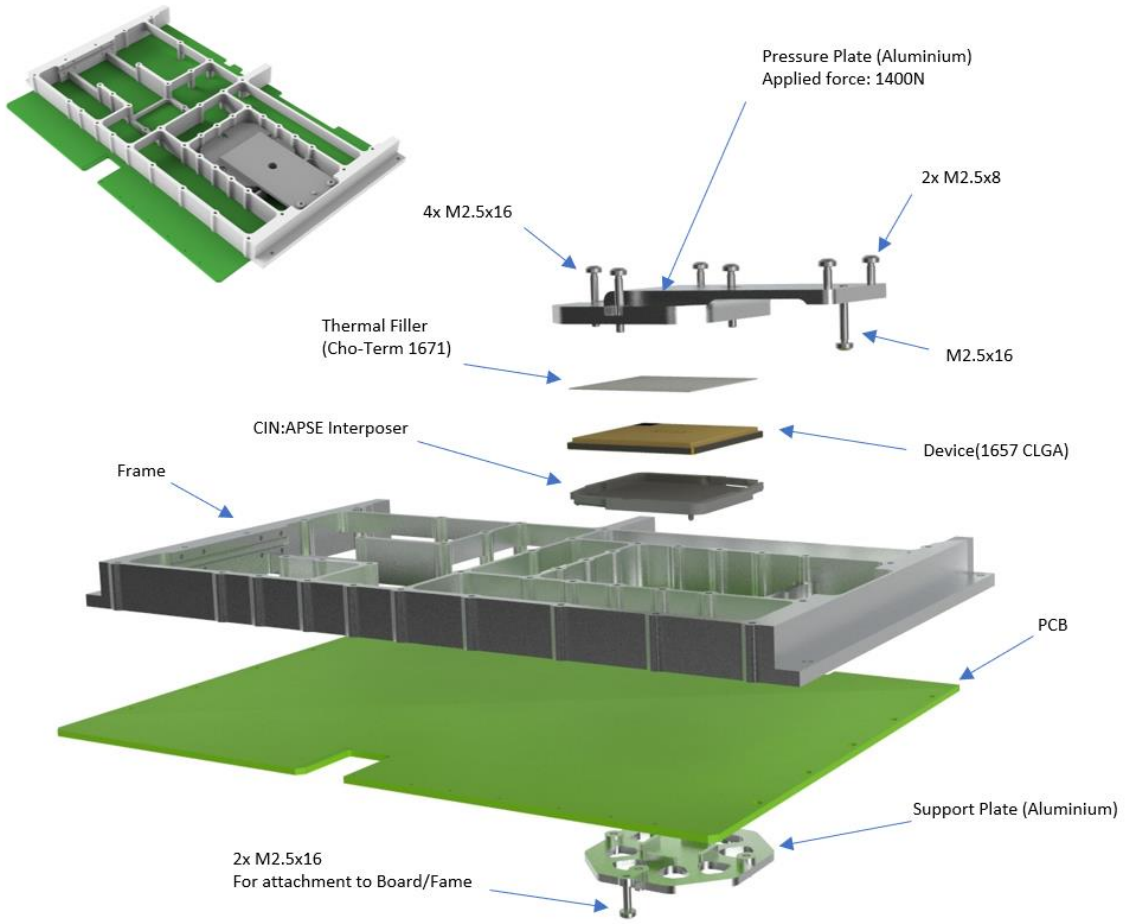
- Backplane communication (cPCIss)
  - 8 x SpaceWire interfaces
  - Redundant CAN Bus
  - 8 x High-Speed Serial Links
  - GPIO for low-speed communication

- Front panel interfaces
  - 2 x SpaceWire interfaces
  - Reserved user IO from FPGA
  - Ethernet/UART Debug Support Unit control interface for test purposes
  - JTAG test and debug
  - PPS (Pulse Per Second) input for synchronization with external time reference



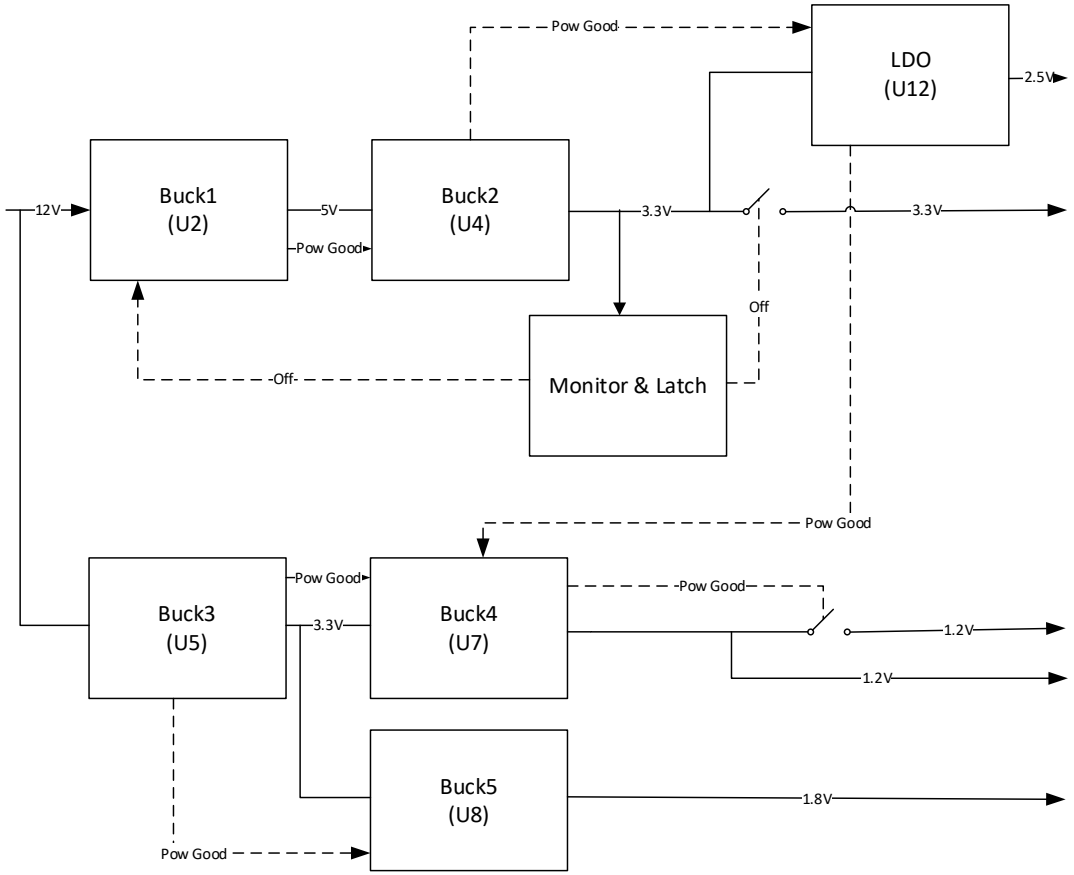
RTG4 solderless mounting

- Due to the need for high-speed signaling, Megtron6 is selected for the PCB.
- Increased risk of mismatch in CTE (Coefficient of Thermal Expansion) which results in problems with solder joints and cracks in the circuit body.
- For this reason, a concept with interposer using solderless interconnection is used for the large RTG4 FPGA.
- The FPGA is pressed to the PCB using top and bottom plates. A meshed gold-plated interposer ensures electrical connections.



Power Architecture

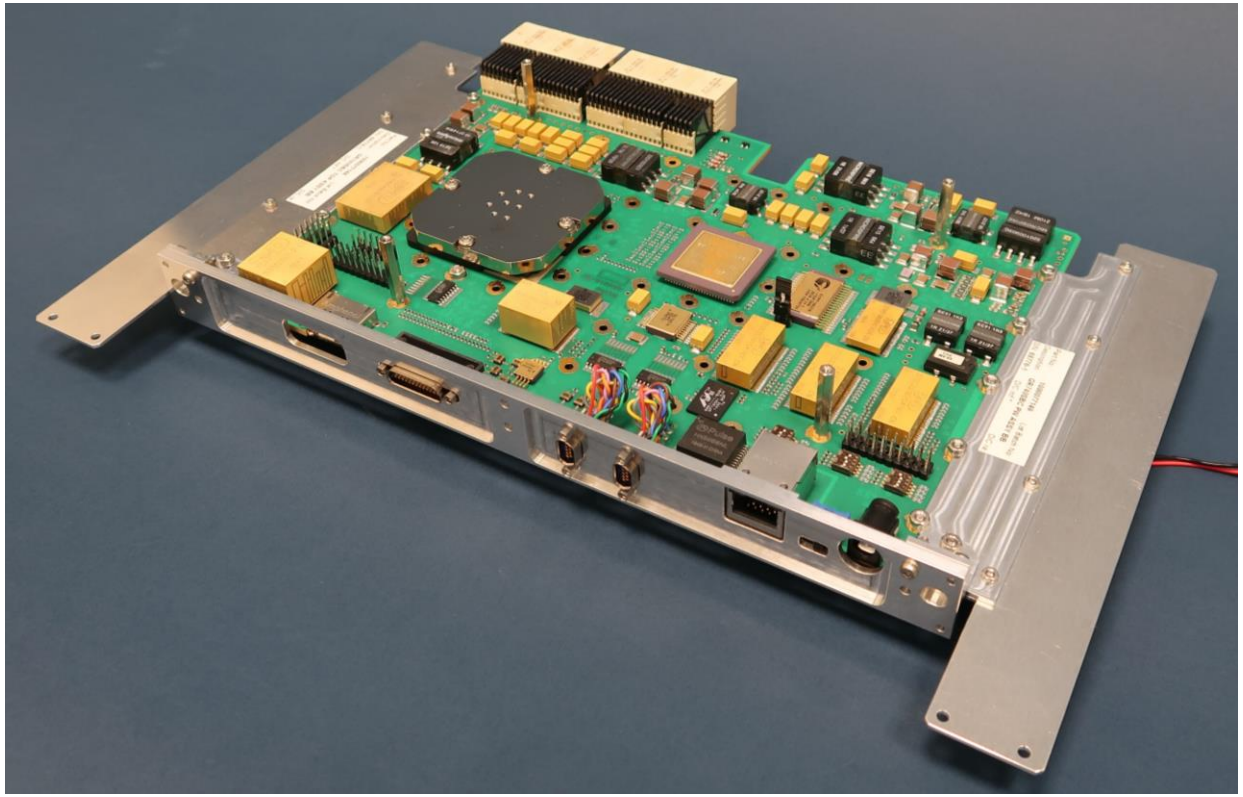
- VIN power input +12V via backplane
- 2-step conversion is selected to prevent failure propagation.
- On-board regulators converting from VIN to 3.3V, 2.5V, 1.8V & 1.2V
- Power consumption: ~30 W
  (worst case estimate, also assuming 100 % FPGA utilized)



Elegant Breadboard

- An Elegant Breadboard has been manufactured and tested successfully.

- Functional tests for memories and interfaces has been performed, including:
  - 1553
  - SpaceWire
  - UART
  - CAN
  - On board memories (SDRAM, SPI flash, MRAM)
  - PCI
  - Ethernet
  - GPIO
  - JTAG
  - FPGA DSU UART



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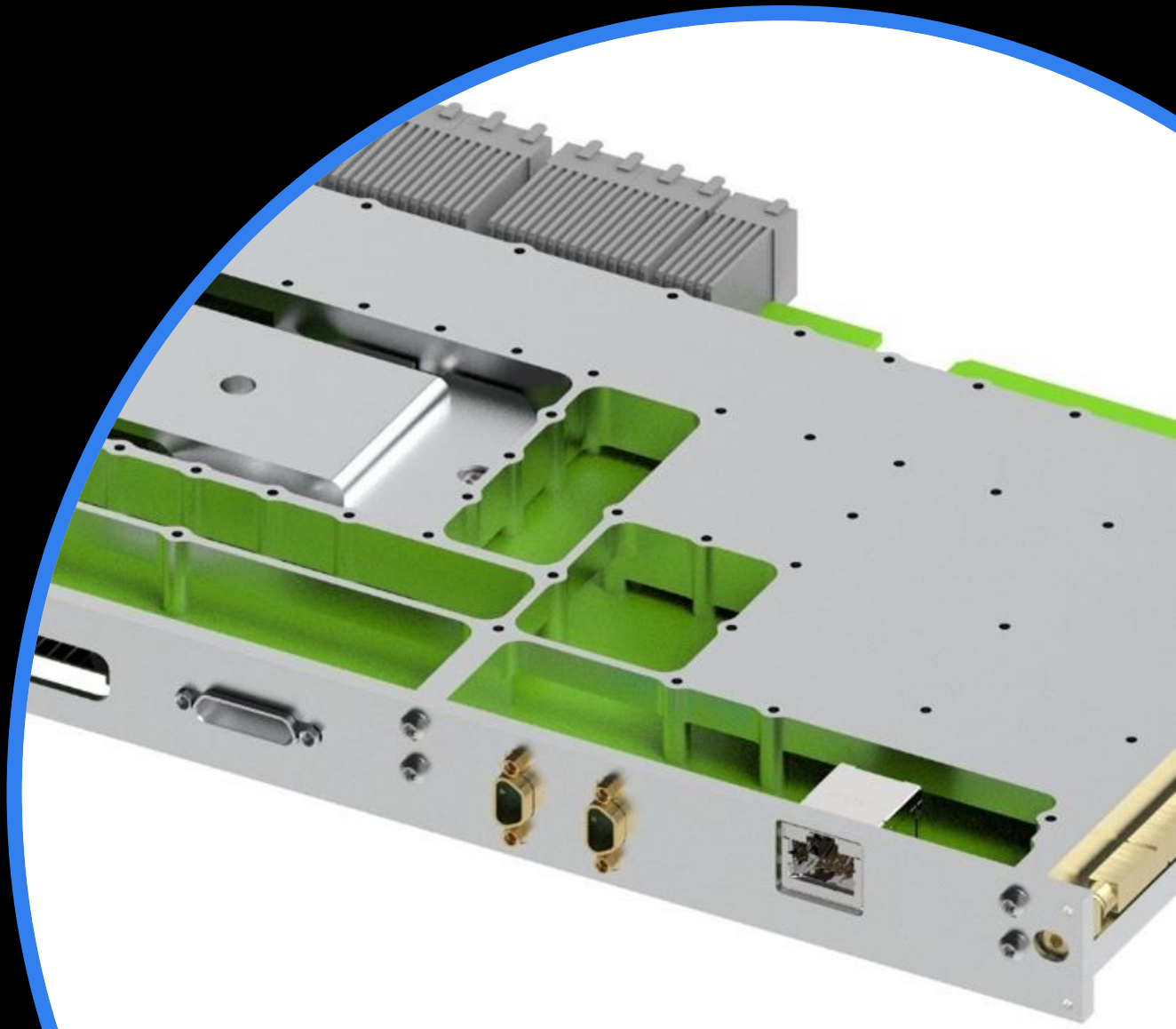
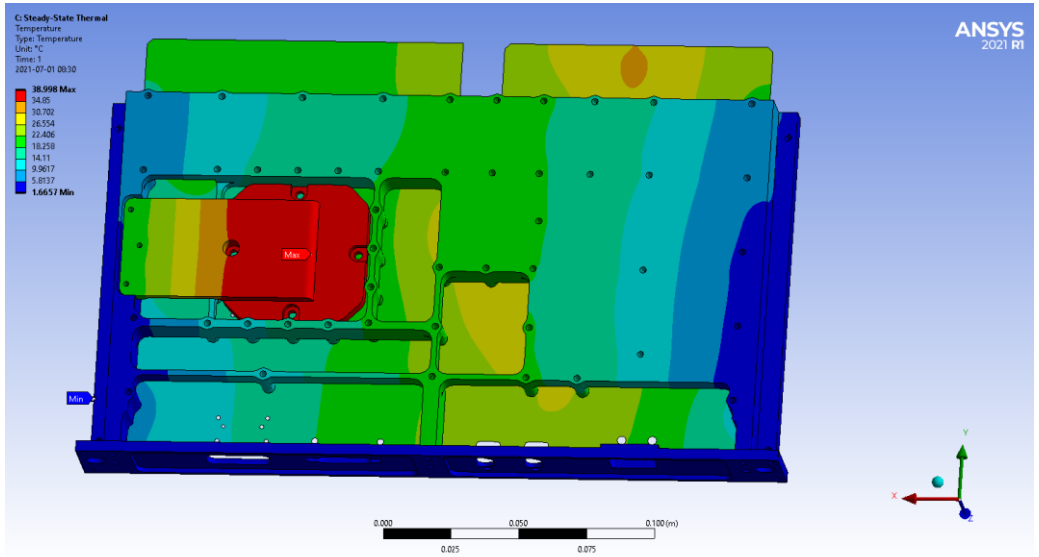
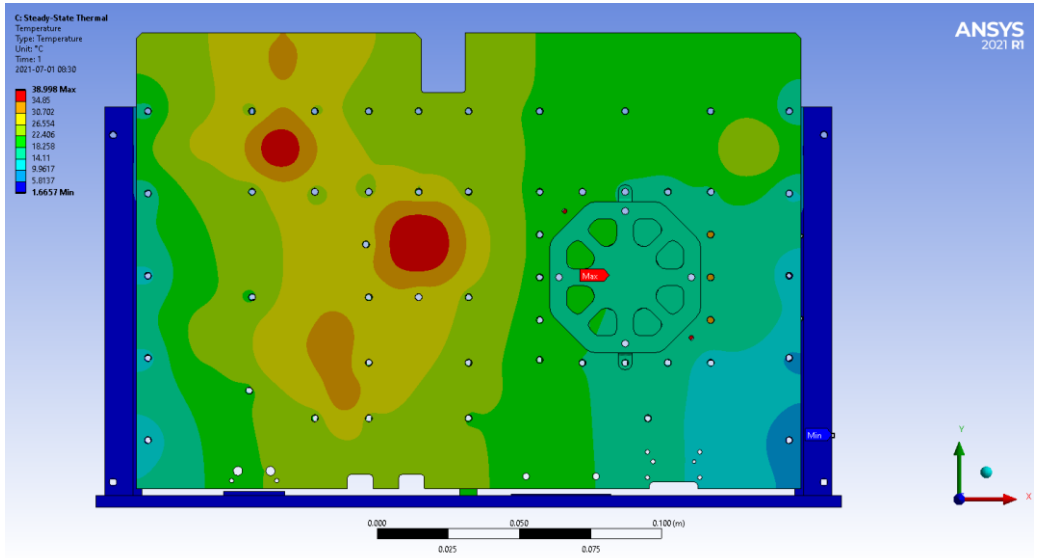
Results and Design Analyses



Thermal Design

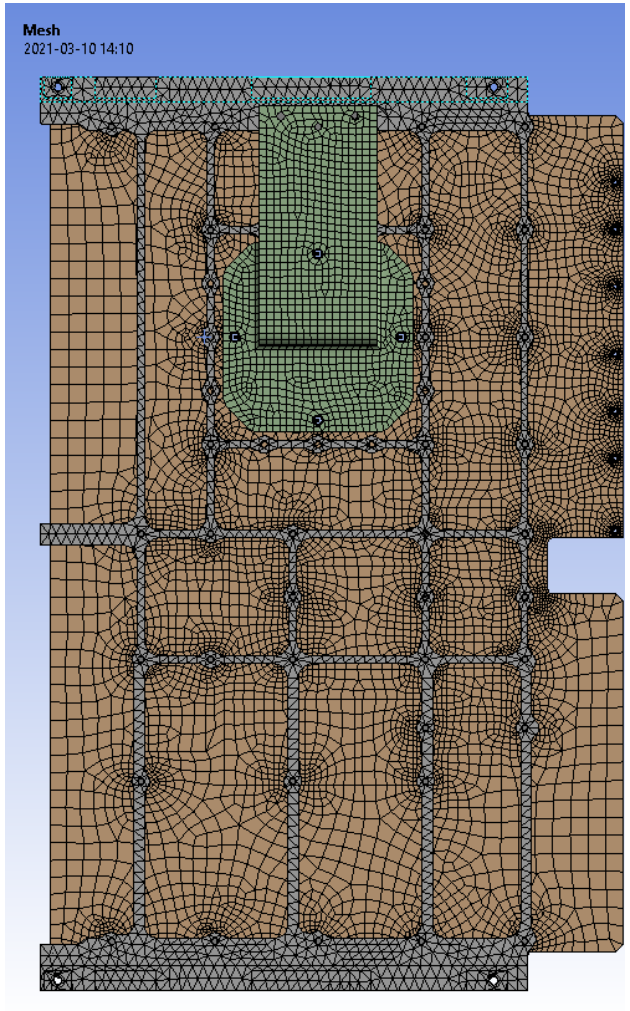
- The SBC is designed with conduction cooling.
  - Thermal bar on the solder side of the PCB and wedge-lock on the component side.
  - The heat transfer is secured via the wedge-lock and thermal bar to the unit crate.
  - The GR740 ASIC is cooled through the pcb to the frame.
  - RTG4 provided with heat sink mounted on frame
- RTG4 and GR740 dissipate most heat
- Analysis/simulation based on worst case scenario with a total power dissipation of 30.5 W.
- Highest board temperature is 38 degree above bord edge (wedge-lock).

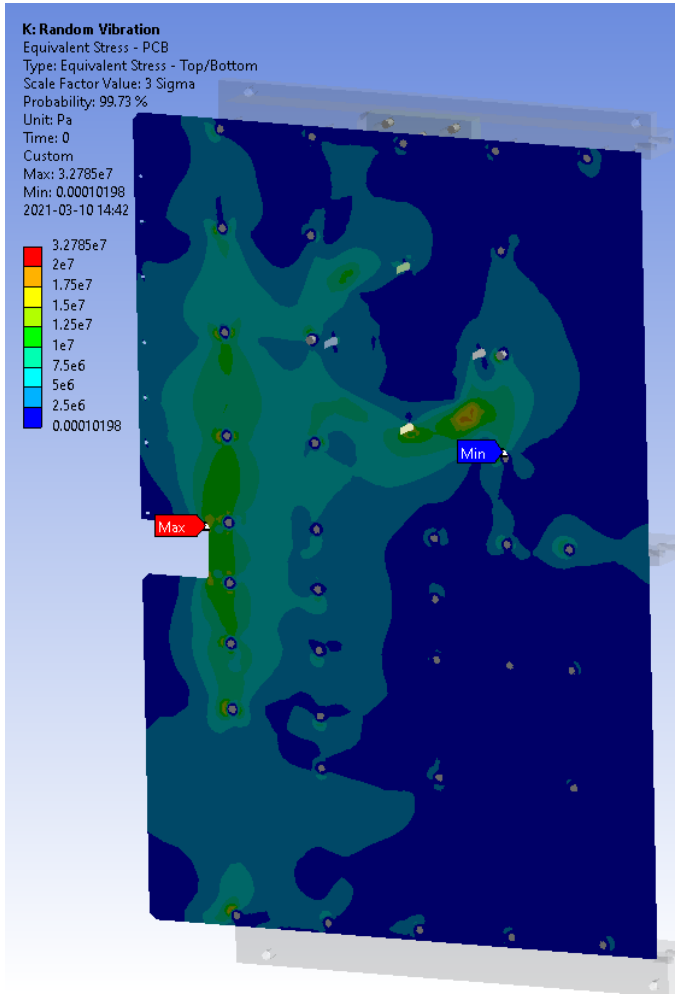




Other Analysis

- Structural Analysis successfully performed.
  - Requirements for stiffness, quasi static loads and random vibrations are OK.
- Worst Case Analysis including for example: timing analysis for SpaceWire, SDRAM and PCI interfaces.
- Reliability Analysis
  - Baseplate temperature 30°C results in 1002,8 FITS

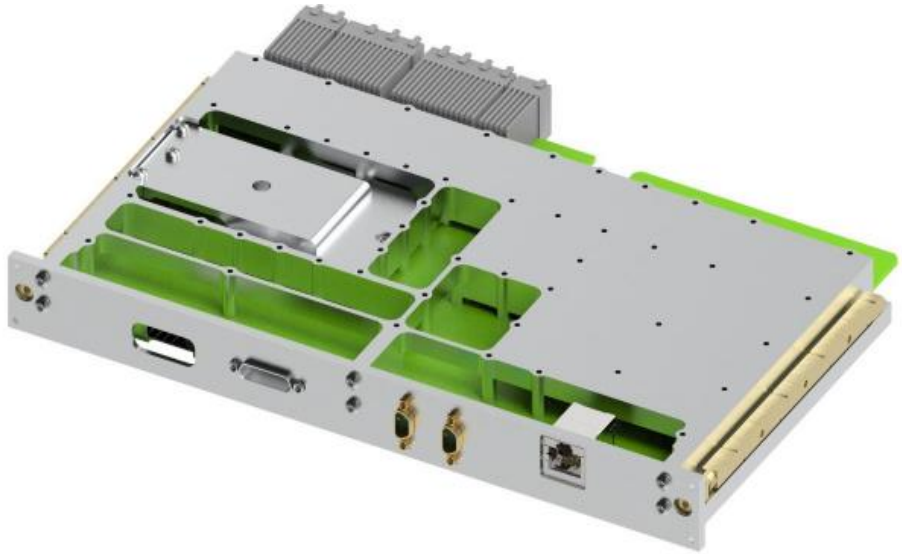




GR740 SBC Reference Design Data Package

- Design data package for Flight Model available for download:

  www.gaisler.com/gr740_sbc_refdesign



HW Design Description	HW Detailed Design Document
User Manual	Reference Design User Manual
	FPGA Detailed Design/User Manual
	GRBOOT LEON boot loader for GR740SBC Overview
	GR740SBC RTEMS driver User Manual
Analysis reports	Worst Case Analysis (WCA)
	Board Parts Stress Analysis (PSA) Report
	Reference Design Radiation tolerance
	Reference Design Thermal Analysis
	Reference Design Structural Analysis
	Reliability Analysis
	GR740 SBC FMECA

Schematics	Reference Design Schematics
PCB layout	Reference Design Assembly Layout
Bill of materials	Reference Design EEE Bill of Materials
	Reference Design Top Assembly Bill of Materials
Model descriptions	RTMM (Reduced Thermal Math Model)
	Reduced FEM (Finite Element Method)
CAE files (board and FPGA design)	Manufacturing files, mechanical drawings (frame, stiffeners etc.) design files essential for the manufacturing drawings
	Board (schematics, layout and Gerber files from Mentor Xpedition)
	GR740SBC power calculator
	RTG4 FPGA Pinout details
	FPGA design delivered by ESA

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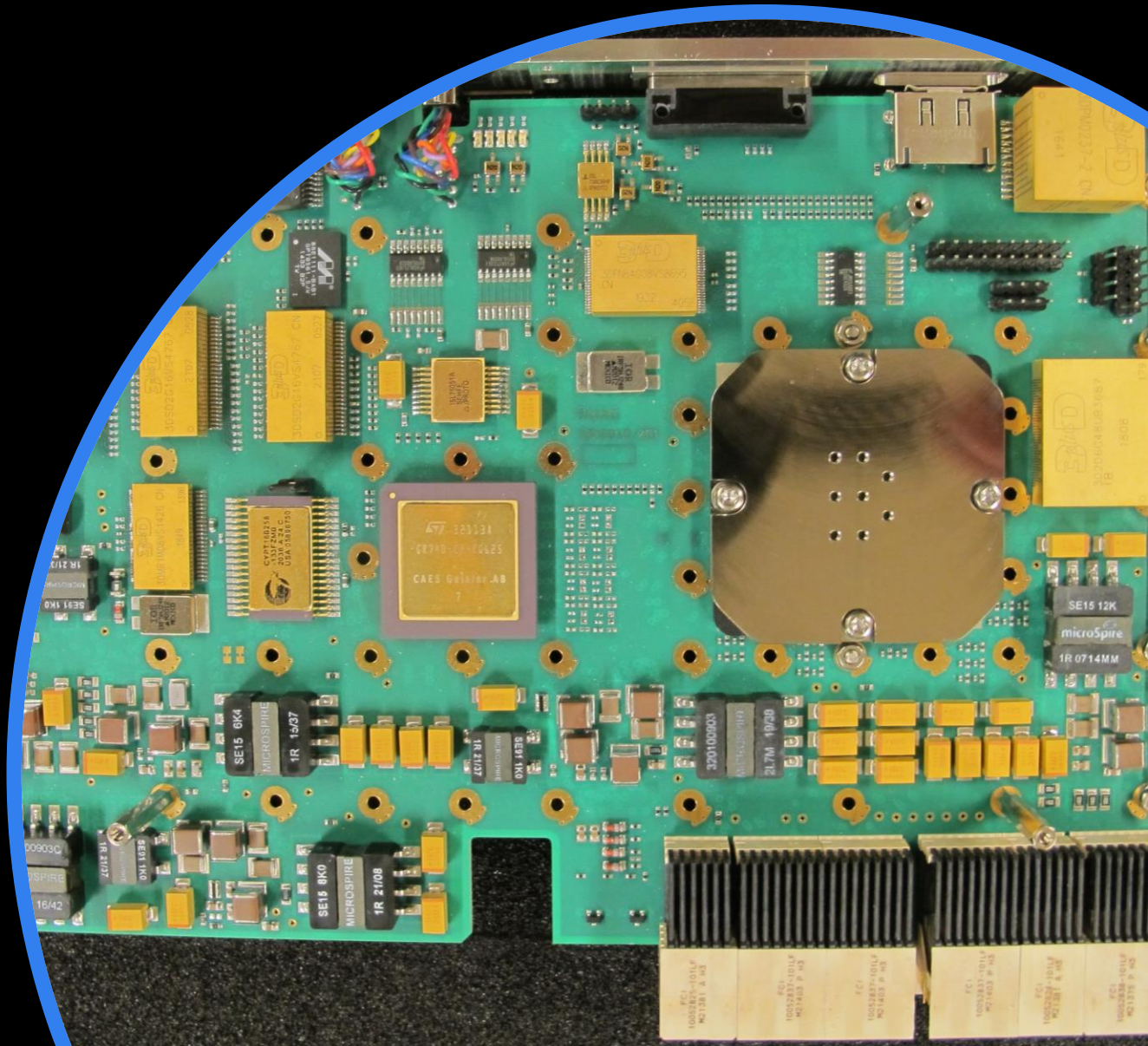
Next step

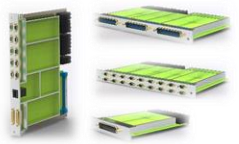


Next Step

- Beyond Gravity will start activities, together with Cobham Gaisler, to further refine the GR740 SBC design and to have a qualified product, **Oryx SBC**.
- The Oryx SBC will be part of Beyond Gravity new product line: Modular Data Handling System (MDHS)
- The Oryx SBC will also be ADHA compliant.

MDHS Product

Core Features
- BG modular system solution
- Compliant with ADHA
- Standardised modules and communication paths
- 6U and 3U units, stand-alone or interconnected



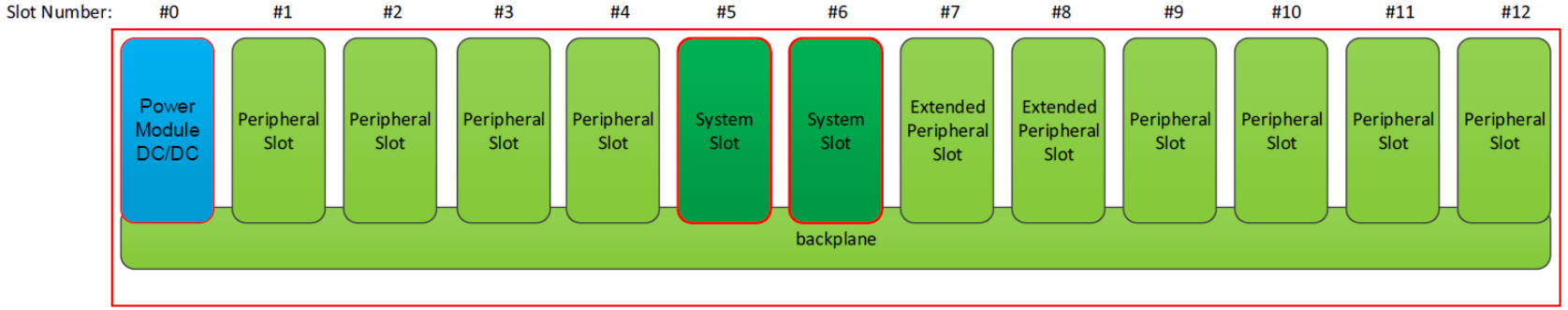
Off-the-shelf Modules
- SBC
- TTR
- DC/DC
- SSMM
- GNSS
- I/O
- …

Many Applications / Units
- **SBC**
- **OBC**
- ICU
- SMU / CDMU
- Payload Processing
- **RTU**
- …

Advanced Data Handling Architecture (ADHA)

- ADHA defines a rack-based system with standardized modules and backplane.
- Cooperation between ESA and industry.
- Based on Compact PCI Serial Space

- Up to 12 slot unit, excluding power module
  - 2 system slots
  - 10 peripheral slots
- System slot supervise and control peripheral and ext. slots.
- Backplane communication:
  - CAN, two busses
  - SpW, two dual stars
  - SpFi, two dual stars



Oryx SBC

- Based on the design developed within the GR740 Reference Design activity.

- Design updated to comply with ADHA.
- Extend number of front panel interfaces.

- Oryx SBC can be used as:
  - SBC in System Slot (system controller)
  - SBC in Peripheral Slot (processing module)
  - On Board Computer together with a second module with Telecommand, Telemetry and Reconfiguration functions.

Technical Summary

- 6U cPCIss
- GR740 Quad Core LEON processor
- RTG4 FPGA
- NAND Flash storage
- Ethernet for debug
- External SpaceWire, M1553 and CAN
- Backplane SpW and CAN.
- SerDes lanes in backplane, prepared for SpFi/PCIe

Thank you for listening!