Airbus Crisa

Next Generation Processing Module for Future Payload Controllers – GR740 Payload Controller Module

CRISA

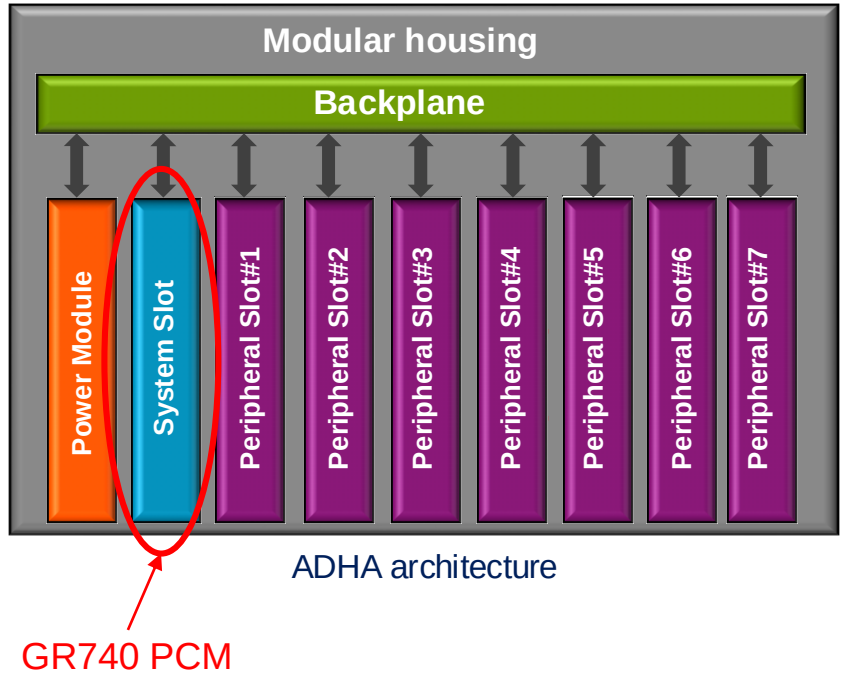
Enrique García Núñez, Technical Manager

13th December 2022

AIRBUS

What is the GR740 PCM?

- The GR740 PCM is a high-performance module based on the multi-core GR740 SoC ASIC and the RTG4 reprogrammable FPGA
- It is conceived as a general purpose Payload Controller Board.
- This module fits in a modular Payload Controller unit architecture
- This board implements the System Slot functionality in the ADHA standard unit.
- Form factor is cPCI Serial for Space 6U.

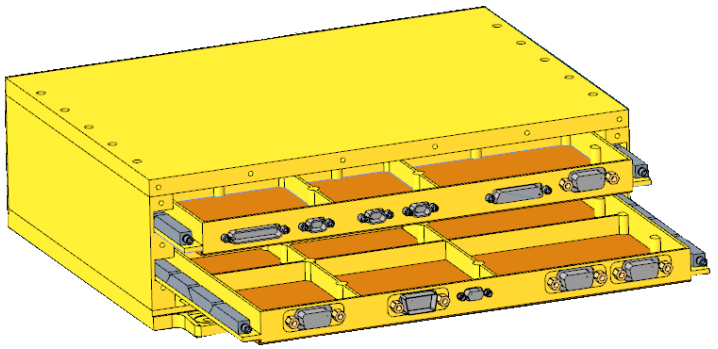


GR740 PCM – Introduction

- Crisa started an internal R&D project by mid 2021 to start the development of the GR740 PCM board

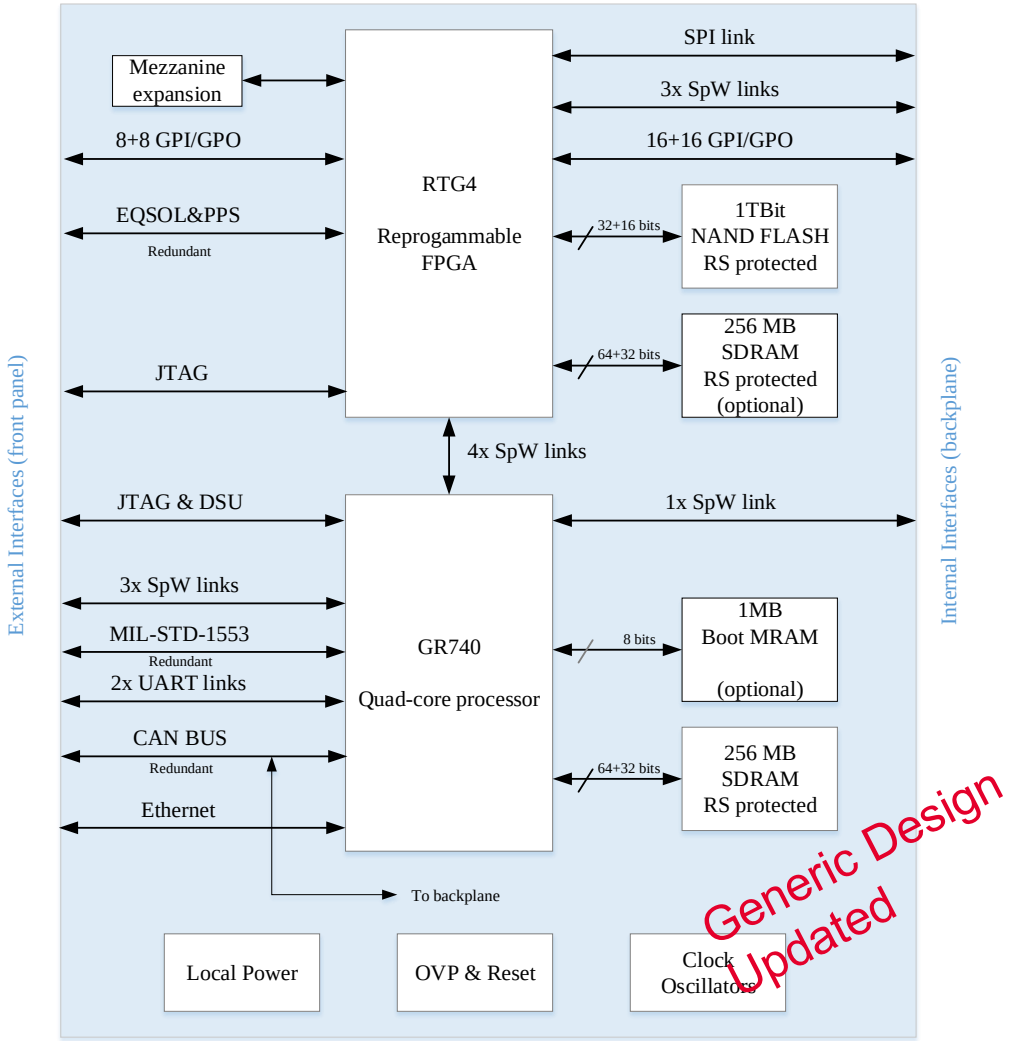
- The design had synergies from PILOT Landing Processing Unit (LPU)
  - PILOT is a suite of advanced landing technologies (hardware and software), enabling global access to the lunar surface, landing precisely and safely
  - It was going to be embarked on Roscosmos Luna-27 lander. PILOT LPU project cancelled.

- After notification of PILOT LPU Project Cancellation, the GR740 PCM R&D was redefined (driven by new ADHA specifications and enhanced performances of the board).

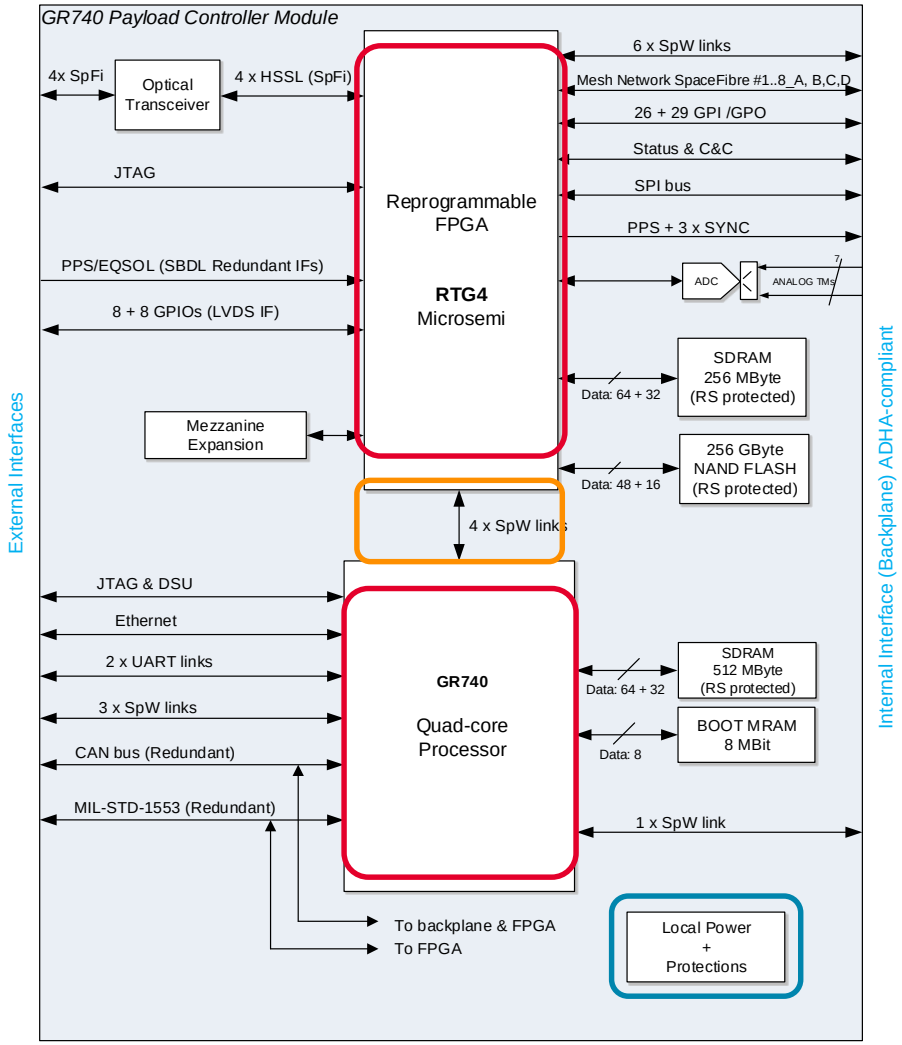


GR740 PCM Overview (before PILOT cancellation)

- Electrical design completed before PILOT cancellation.
- Mechanical concept from ADHA: form factor is cPCI SS 6U with standard depth (160mm) and normalized pitch of 5HP (25,4mm)
- The board presented some deviations wrt to ADHA standard unit with some deviations wrt the standard:
  - Backplane connectors
  - Main internal power distribution done with +3V3 supply
- GR740 PCM design has been evolved with additional performances and fully-compliant to ADHA standard

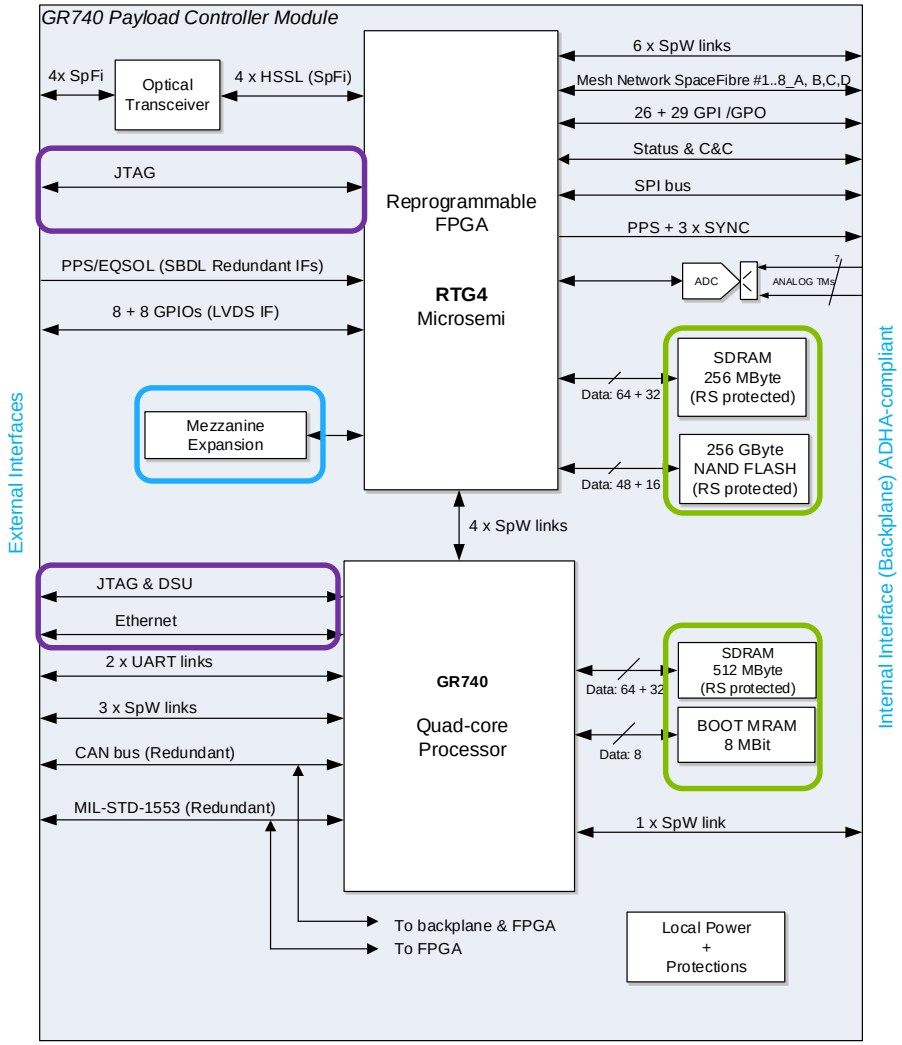


GR740 PCM evolution performances



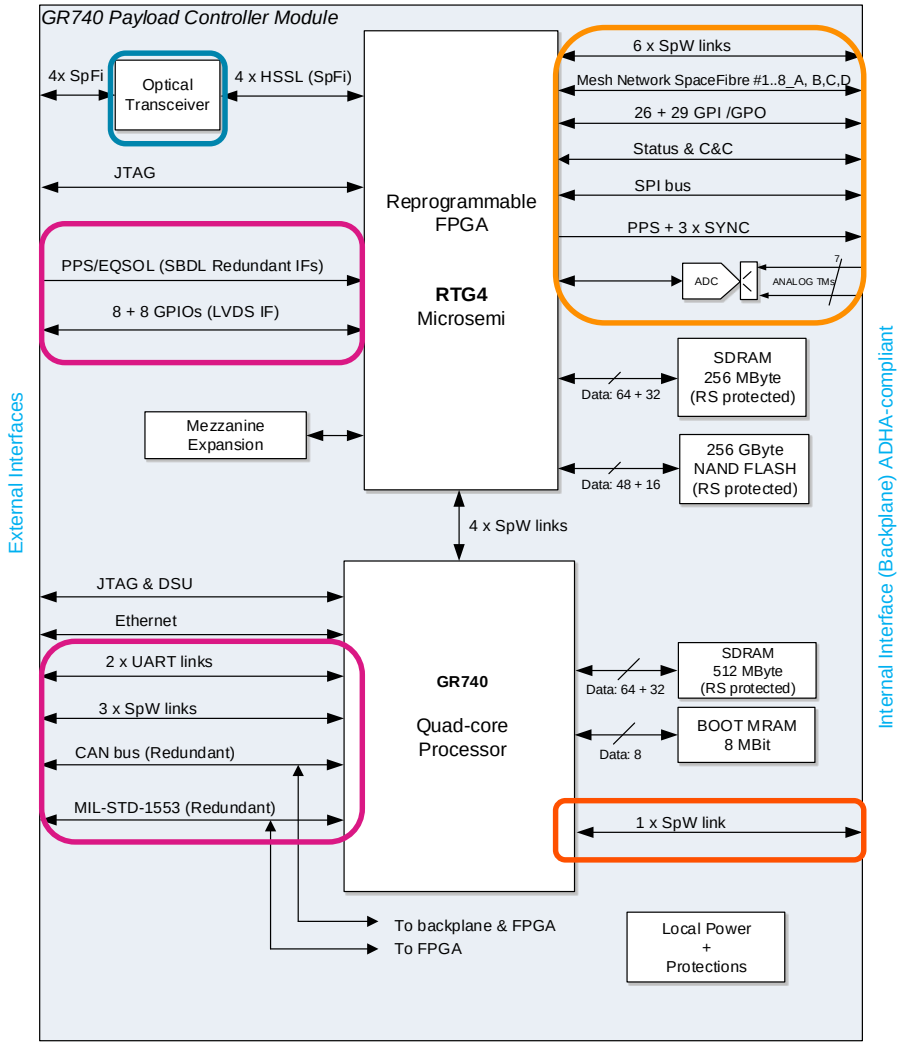
- GR740 Processor (LEON4-FT), processor core running at 250MHz (459 DMIPS single core, 1.744 MIPS aggregated capability for quad cores)
- RTG4 Companion FPGA (Microchip Flash based technology) – Reprogrammable on ground (with unit closed)
- Processor & FPGA connected through 4 x 200Mbps SpW links
- Powered at +12V main secondary power supply
  - Local supply rails generated by POL and LR
  - Overvoltage and LCL protection for external failure propagation avoidance
  - Optionally supplied from +3.3V as a main power supply.

GR740 PCM evolution performances



- Memory banks
  - 1 Mbyte BOOT MRAM memory (optional, for long term storage missions)
  - 256 GByte NAND FLASH NVM for Boot, ASW and Scientific data Mass Memory
  - 512 MByte processor SDRAM bank (RS protected, 64+32).
  - 256 MByte FPGA external SDRAM bank (RS protected, 64+32) - optional
- Extension capability via a mezzanine card
- Debugging interfaces (available in front panel connectors)
  - SW debug interface via JTAG, DSU and Ethernet
  - FPGA bitstream on ground programming via JTAG

GR740 PCM evolution performances



- External interfaces (available in front panel connectors)
  - 3 x SpW interface , 200Mbps, LVDS standard.
  - Dual 1553 bus (BC/RT configurable)
  - Dual CAN bus
  - Ethernet bus (for Debug purposes)
  - Redundant EQSOL & PPS interfaces, SBDL PHY.
  - 8+8 LVDS GPI/O connected to FPGA (functionality mission dependent)
- External interfaces (available in rear panel connectors)
  - High Speed Optical Serial Lines (4 lanes x 3,125Gbps) over SpaceFibre
- Internal Interfaces (available in backplane connectors)
  - 7 x SpW interface, 200Mbps, LVDS standard. For high data throughput slots connection
  - 1x SPI interface, up to 10Mbps (for legacy products)
  - Dual CAN bus. For low data throughput slots connection
  - 26 GPIs+29 GPOs connected to FPGA (mission dependent)
  - Analog telemetries acquisition function
  - 8 + 8 HSSL SpaceFibre mesh network

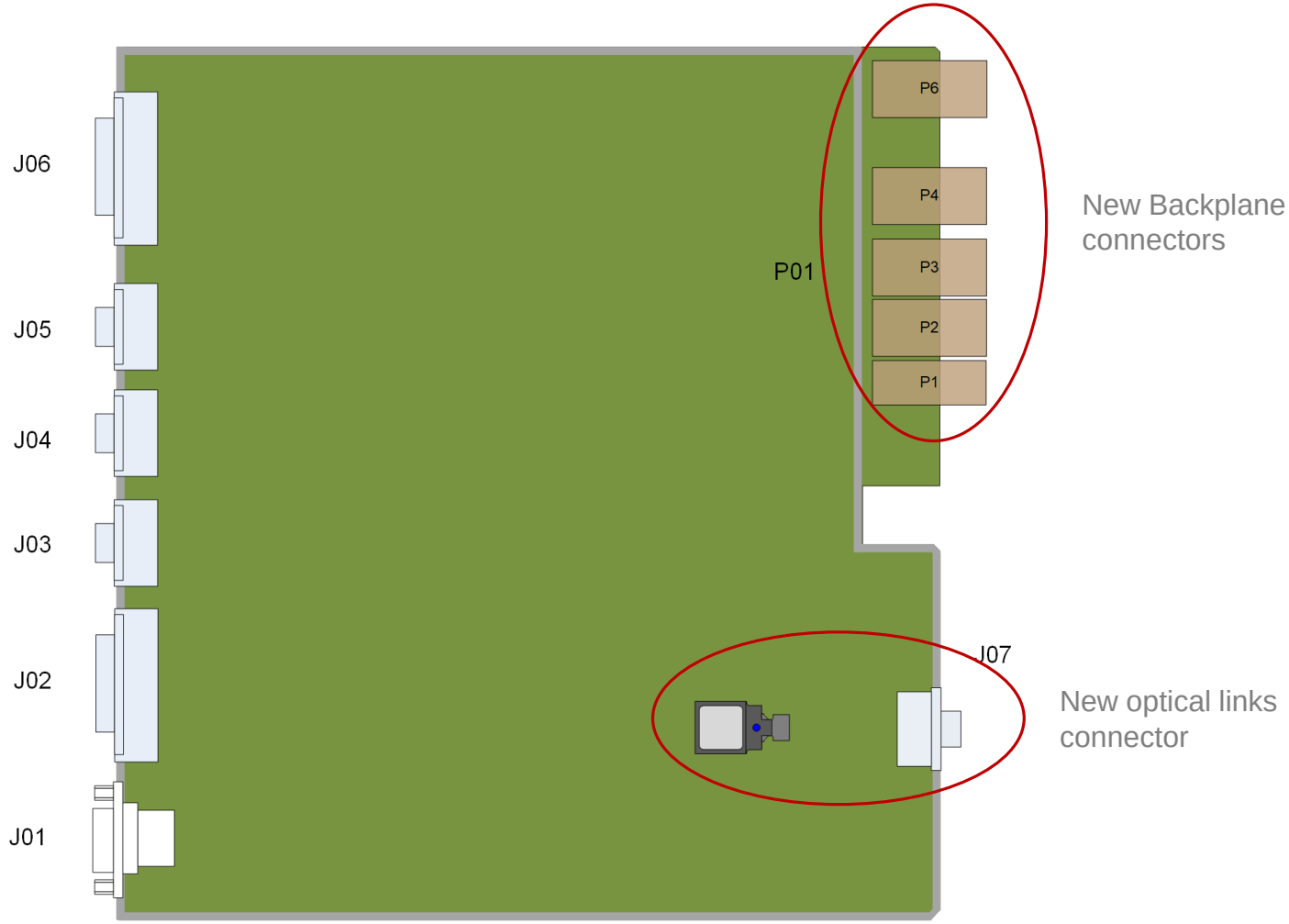
GR740 PCM evolution

- cPCI SS 6U with extended depth (220mm) and normalized pitch of 6HP.

- Front panel interfaces:
  - 1x MIL-STD-1553
  - 3x SpW links
  - 8+8x GPO/GPI LVDS/SBDL lines
  - Debug & Utility connector
    - Dual CAN bus
    - Dual UART link
    - Redundant PPS/EQSOL
    - Ethernet for debugging
    - JTAG for FPGA bitstream upload

- New backplane connector (compliant with ADHA standard)

- New rear panel connector for optical links



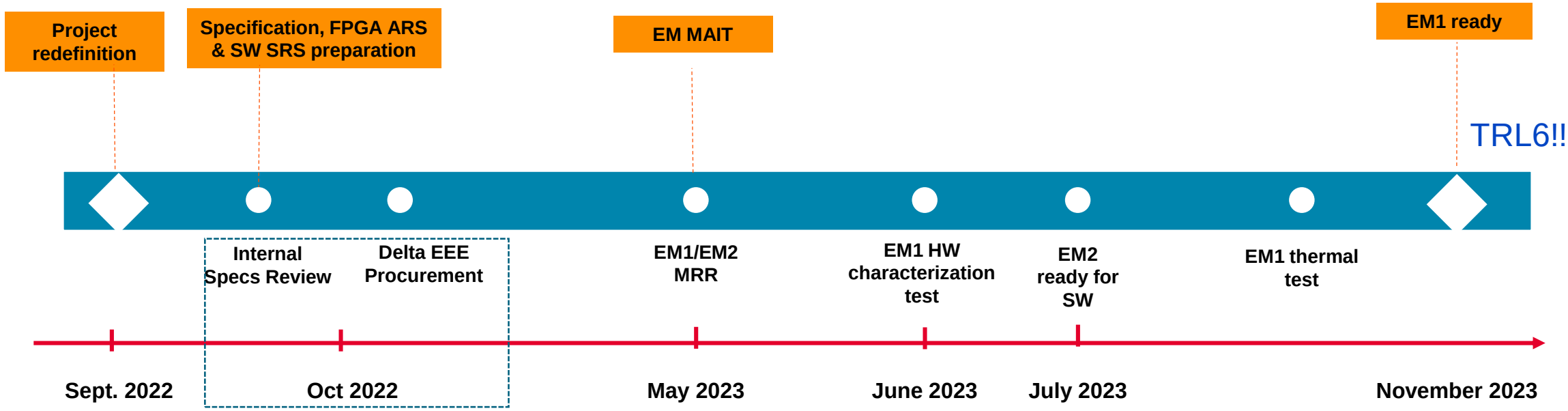
GR740 PCM R&D: Airbus Crisa Plan

- The GR740 PCM R&D plans to submit the first EM to full characterization testing (including thermal cycling) to reach TRL6.

- FPGA design: currently developing the required functionality in the FPGA for board operation and full characterization:
  - Boot control
  - Mass memory controller
  - Other functions required for the application (HSSL, time datation function, etc.)

- SW design: SW for board operation and full characterization:
  - Initialization routines (self-check and ASW loading)
  - HDSW (module drivers, including GR740 processor)
  - Other functions required for the application

GR740 PCM R&D: Airbus Crisa Plan



Thank you