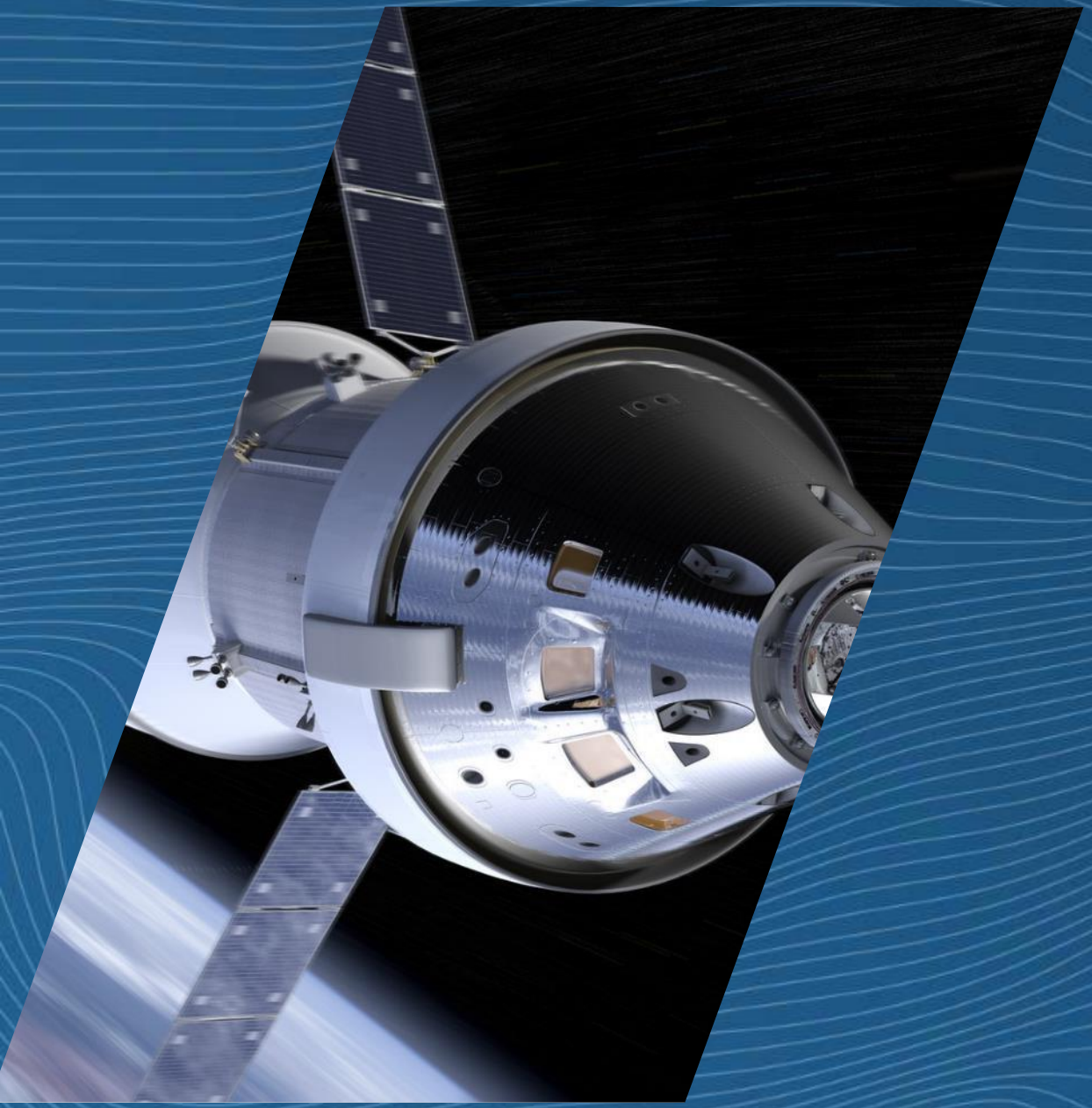


CAES PIONEERING ADVANCED ELECTRONICS

# GOMX-5

## Advanced Payload Processors (APPs)

## GR740 User Day

Gustav Olofsson

2022-12-13

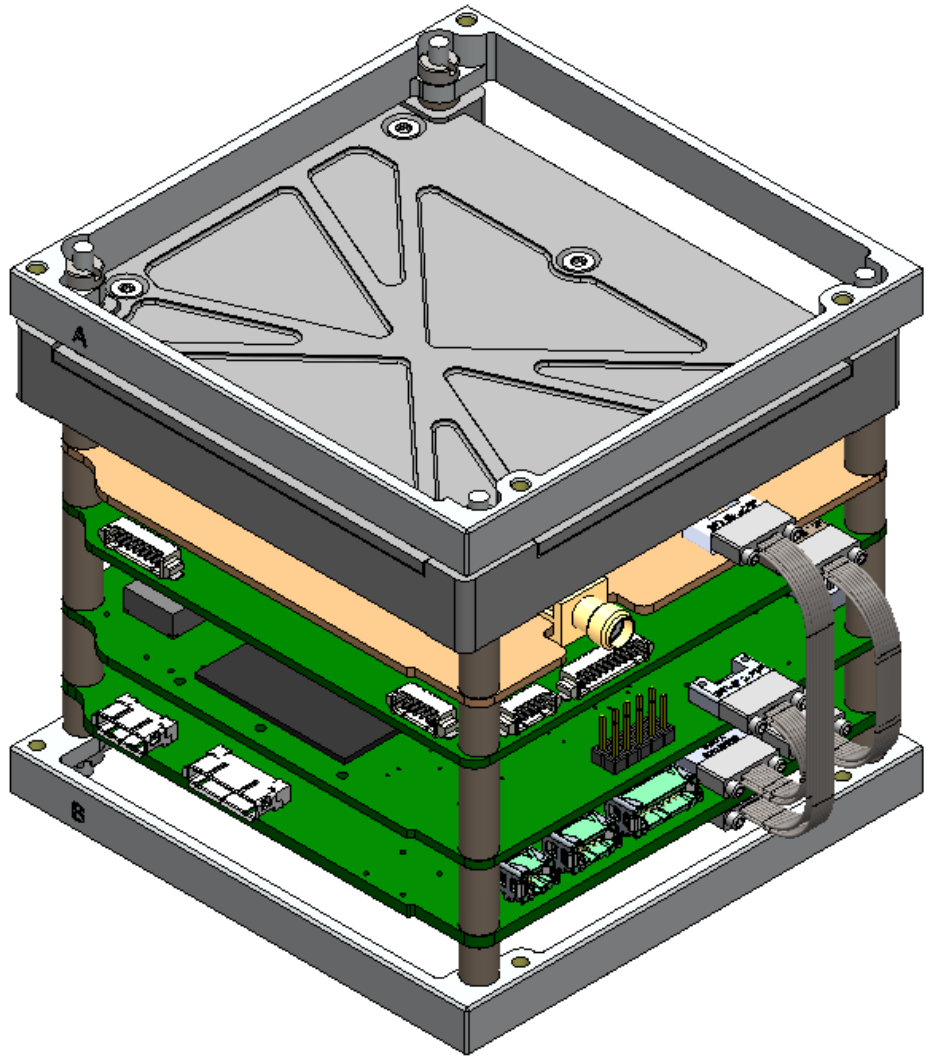
# Agenda

- Introduction
- APPs design
- GR740 system design
- Objectives and experiments
- Test campaign
- Conclusion

# Introduction

## Main objective

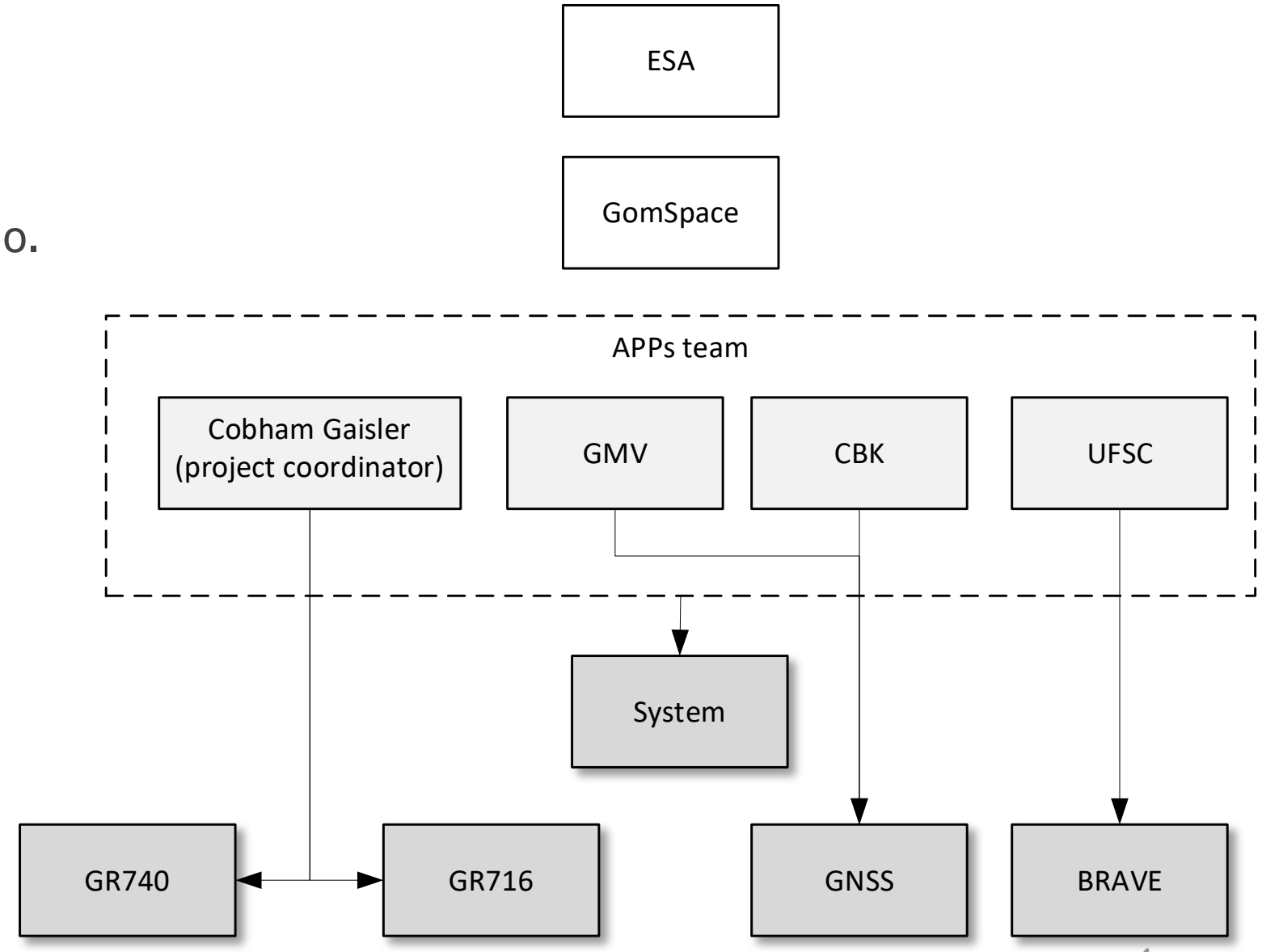
- Demonstrate multiple processing technologies developed within ESA activities and acquire flight heritage from related components
- By means of
  - Combination of processors and reconfigurable logic in APPs allowing for multiple IOD experiments.
  - Realization in the Advanced Payload Processor (APPs) 1U size payload module



# Introduction

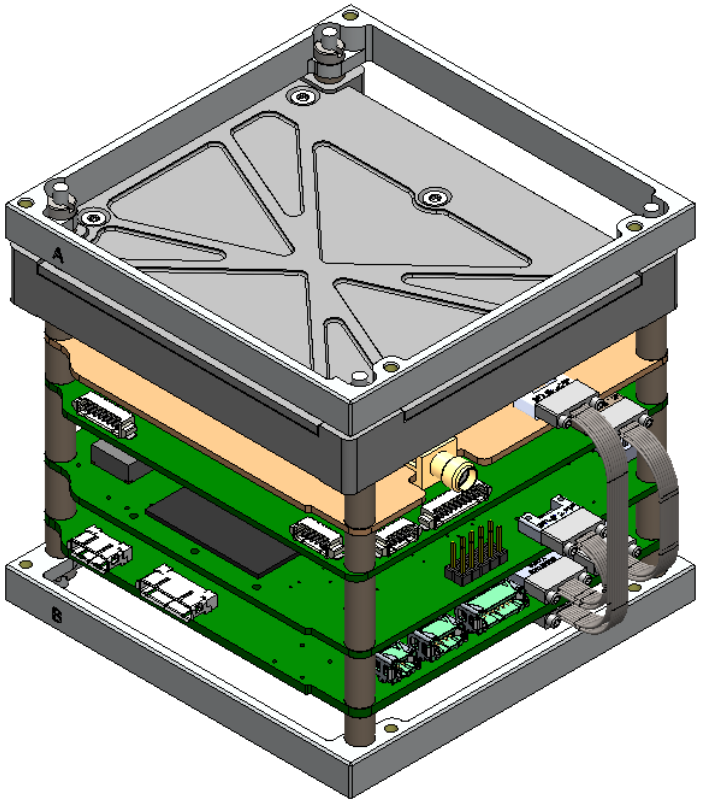
## Consortium and responsibilities

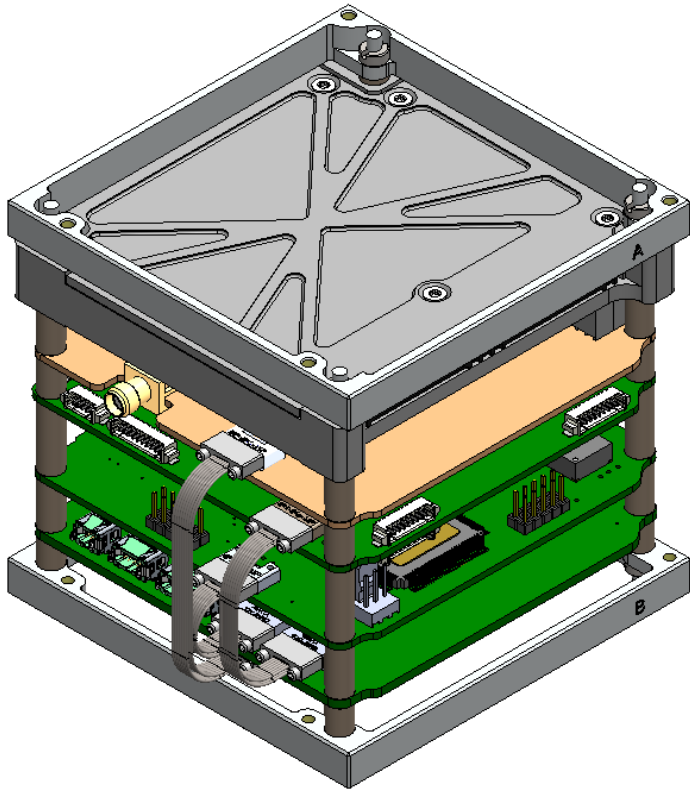
- Cobham Gaisler AB, Göteborg, Sweden
- CBK PAN, Warsaw, Poland
- GMV Innovating Solutions Sp. z o.o. Warsaw, Poland
- Space Technology Research Laboratory, UFSC, Florianópolis, Brazil

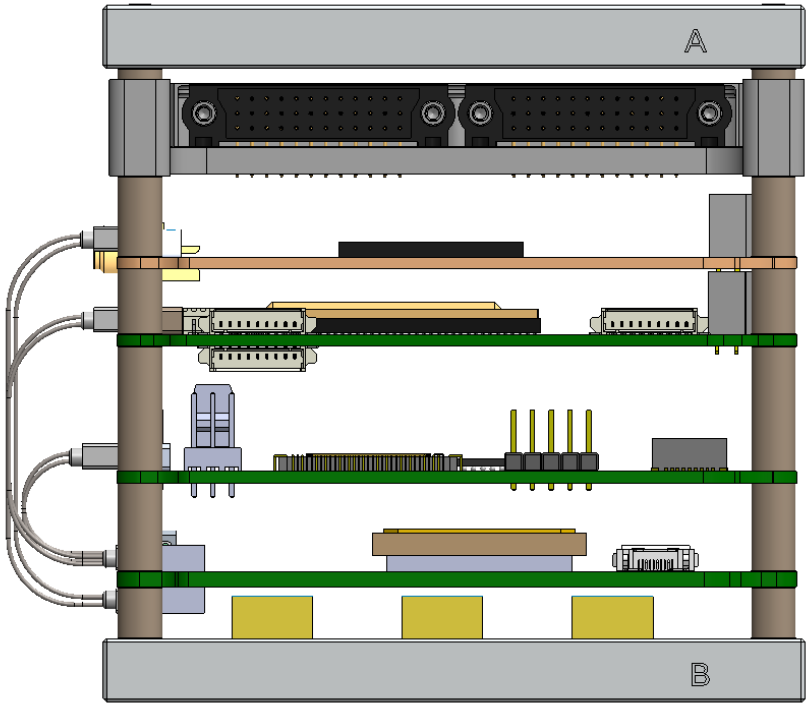


# APPs design

## Five stacked boards



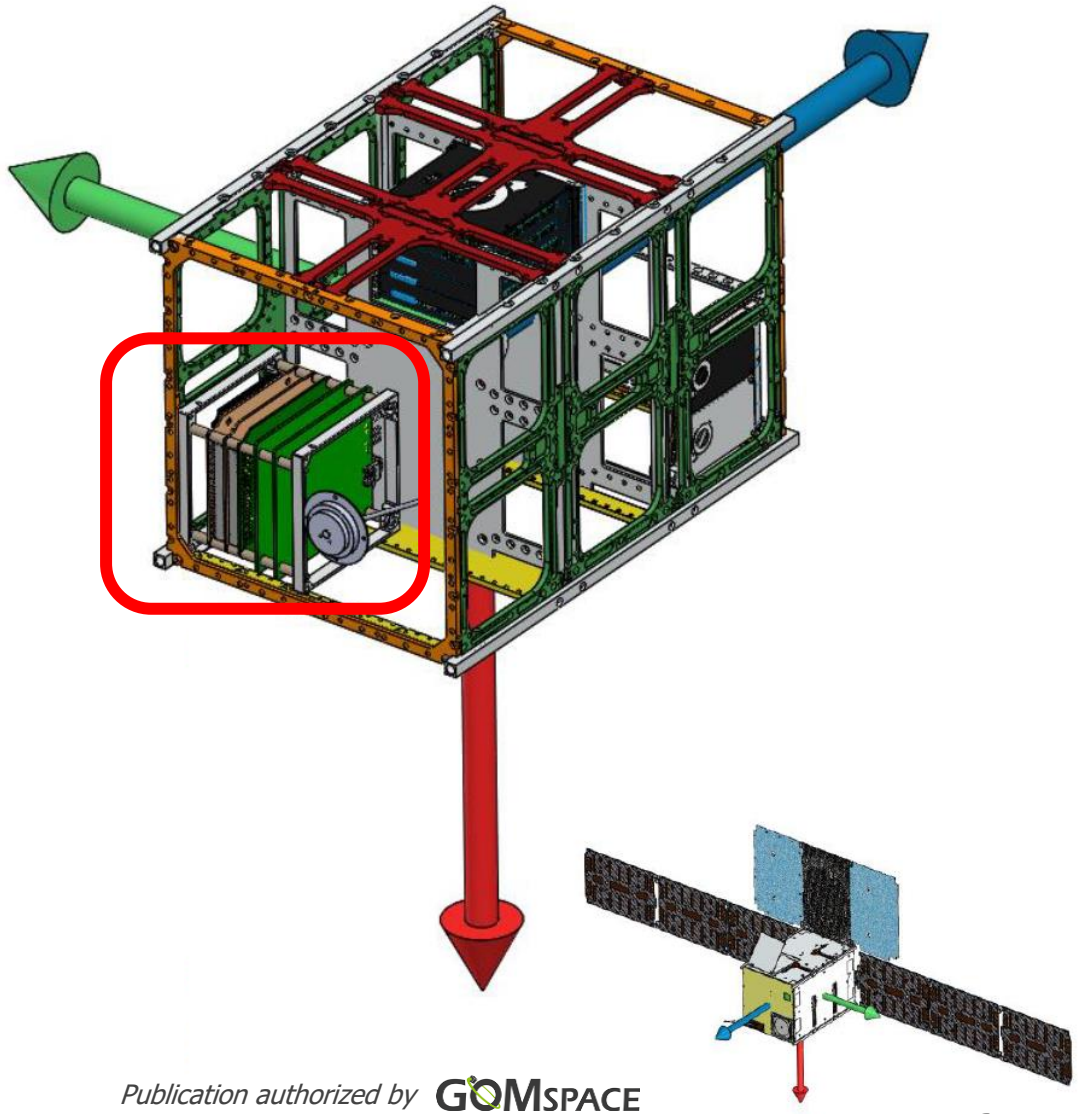



# APPs design

## Spacecraft integration

Integrated as a 1U module in the 12U GOMX-5 satellite developed by Gomspace

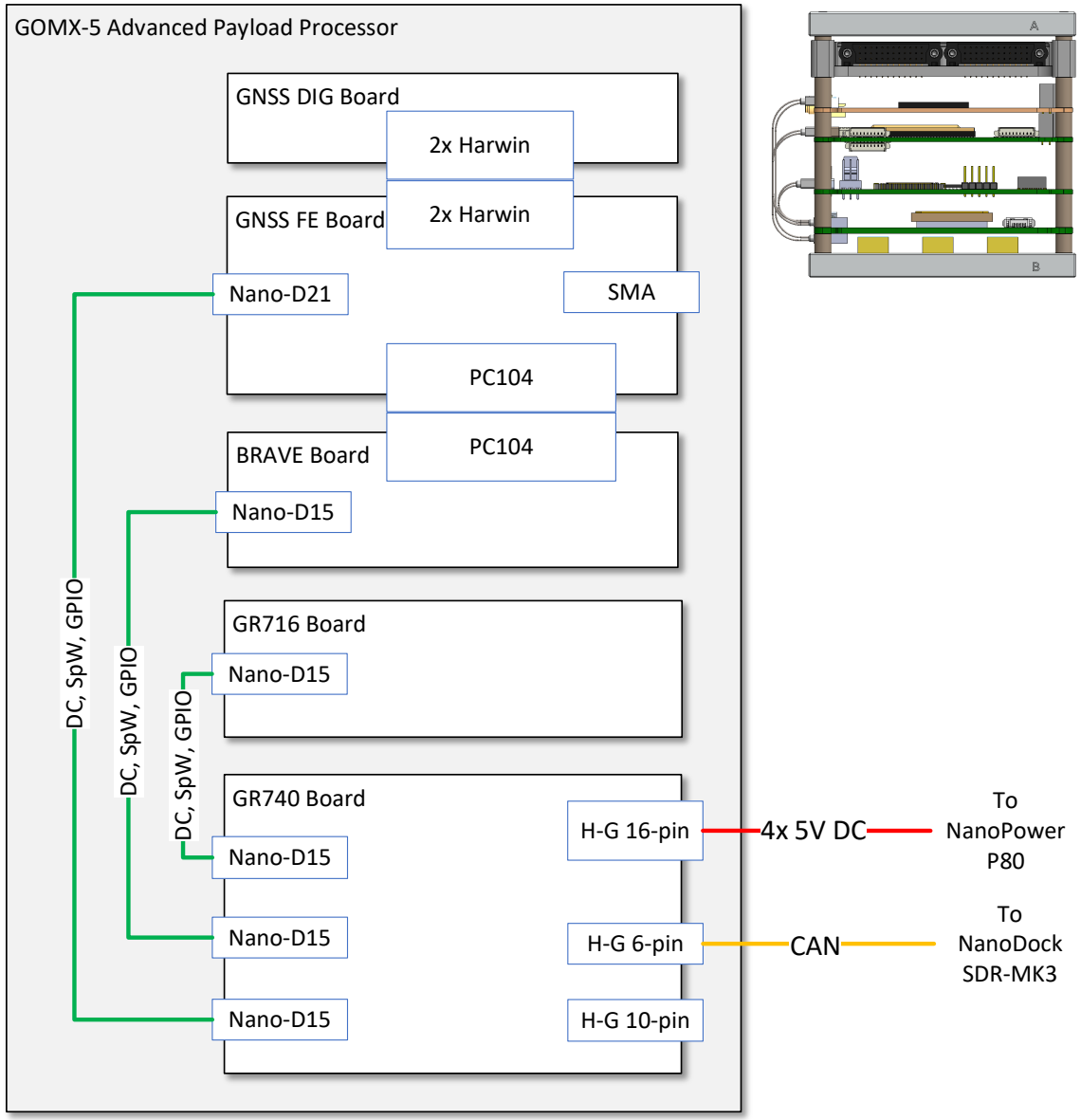


GOMX-5
ENABLING THE CONSTELLATIONS OF TOMORROW

*Publication authorized by* GOMSPACE

# APPs design

## Main functionalities of the boards





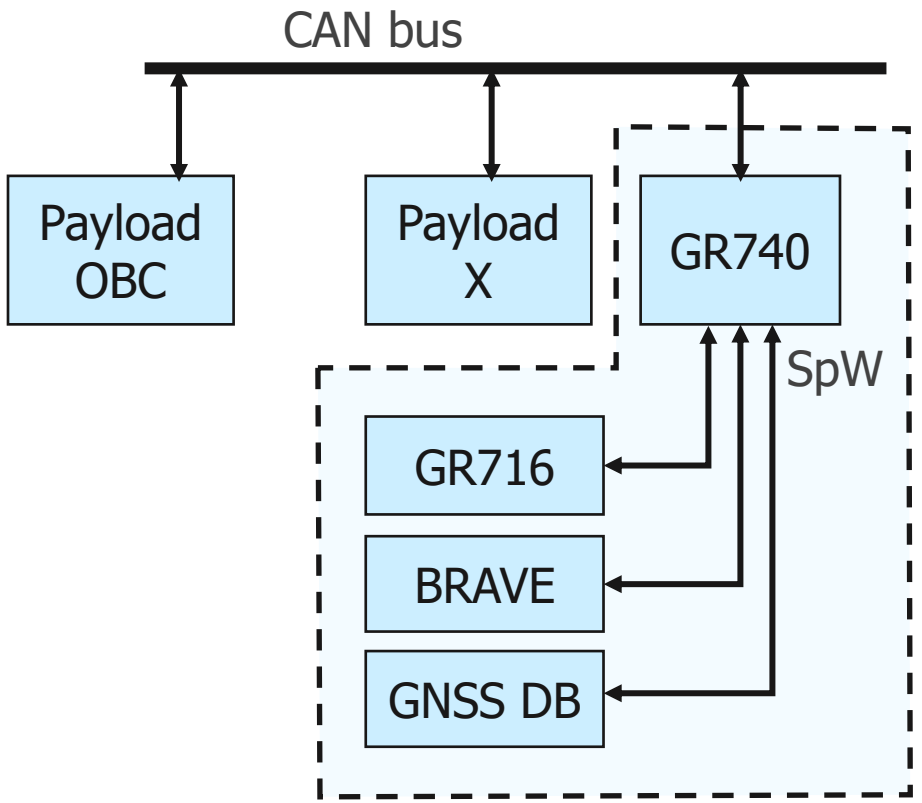

- GNSS Digital
  - Processor part of GNSS Software Defined Receiver
- GNSS RF Frontend
  - RF frontend part of GNSS Software Defined Receiver
- BRAVE
  - Reconfigurable NG-Large FPGA supported by microcontroller
- GR716
  - Microcontroller accompanied by co-processor (LEON5/NOEL-V demonstrator) and radiation sensors
- GR740
  - APPs cube controller, power and communication router
  - High performance processor, runs experiments on unused processor cores

# APPs design

## Communication with payload OBC

**Network interface to payload bus**

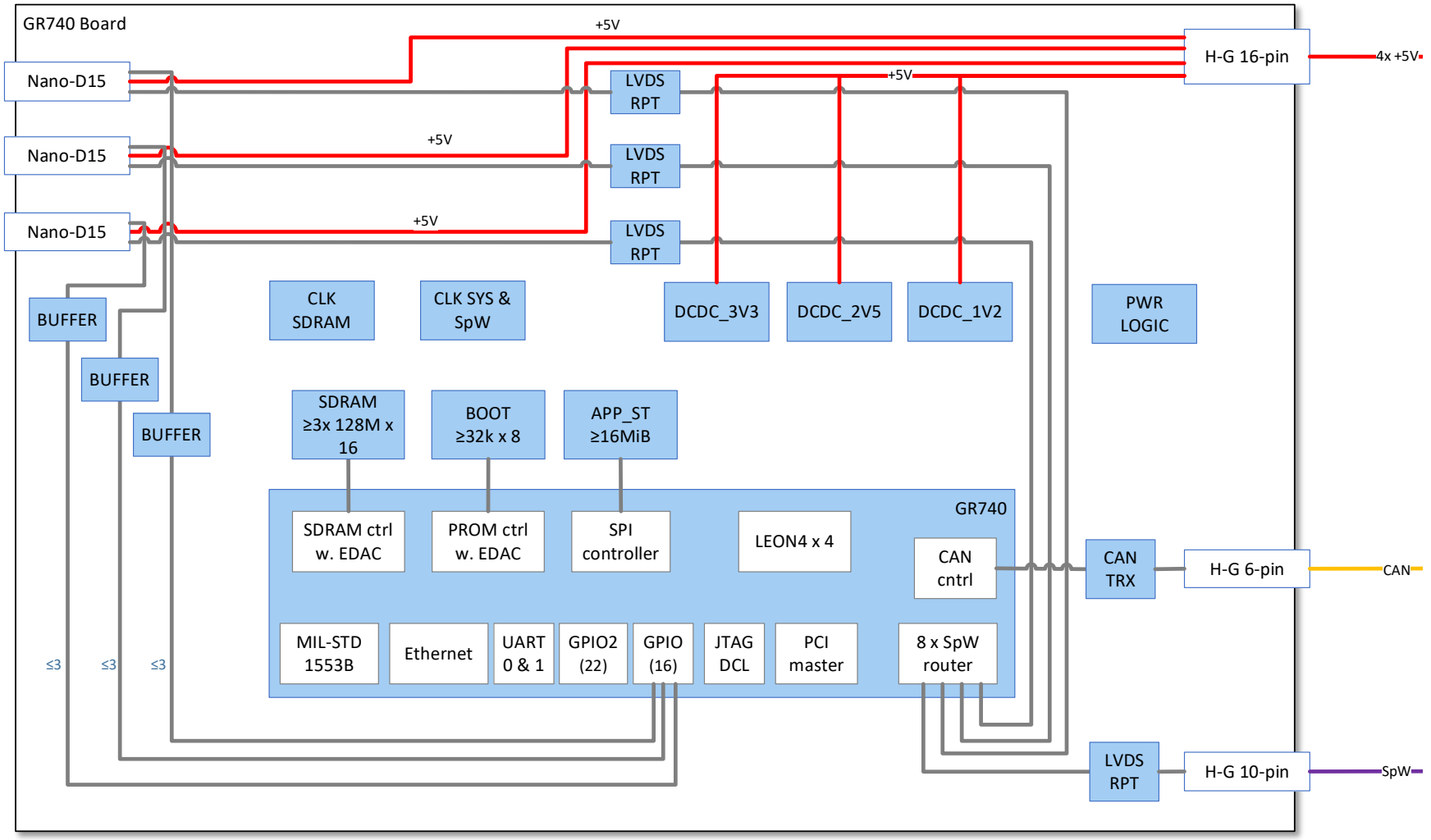
- GR740 provides main communications interface to APPs
- CSP used as TM/TC protocol
  - The Cubesat Space Protocol (CSP) is a small protocol for communication between distributed systems in smaller networks, such as Cubesats.
  - CAN bus used as the physical communications layer on the GOMX-5 platform
- Protocol ported to RTEMS 5.1 Operating system used in application
- Uses the GR740 RCC 1.3.1 GRCAN driver for the CAN interface
- Supports standard CSP services
  - Memory read/write
  - Ping
  - Telemetry request
  - Reboot
- Services have been added to allowing for:
  - APPs systems board management
  - Routing of commands to individual boards
  - GNSS Zynq application update
  - GR716 RMAP interface, provides application updating and debugging
  - GR740 flash interfacing

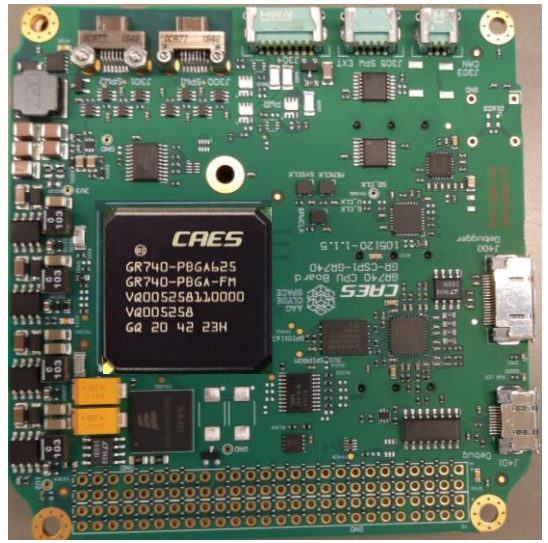


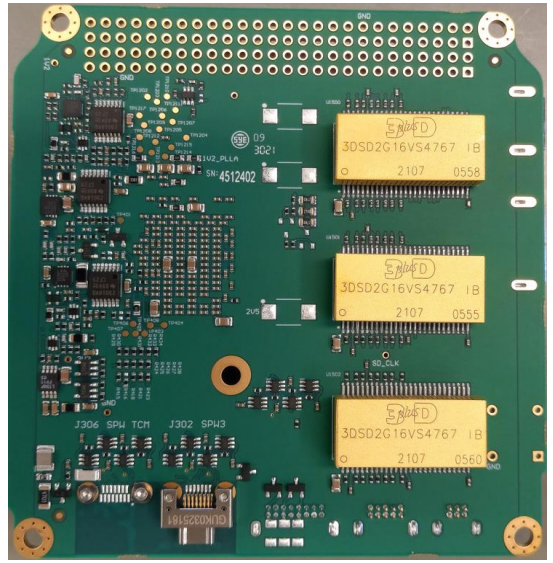

*APPs Network interface*

# APPs GR740 board

## Architecture and realization



# APPs GR740 board

Main component

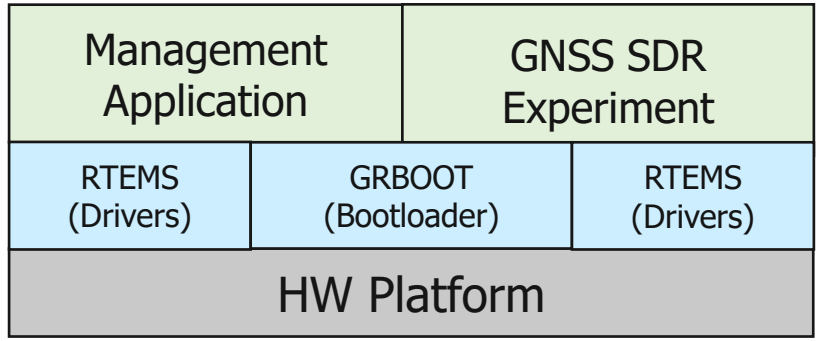
## GR740-PBGA - Quad-Core LEON4 SPARC V8 Processor

- Plastic version of the radiation-hard quad-core fault-tolerant LEON4 SPARC V8 processor targeting space constellations
- Same functionality, fault-tolerance and radiation-hardness as the GR740 system-on-chip device in ceramic package
- Two quality and temperature ranges
  - GR740-CP-PBGA625 - prototype quality, commercial temperature range
  - GR740-AS-PBGA625 - flight quality (ESCC-Q-60-13C class 2), automotive temperature range -40C to +105C
- Developed within ESA ARTES Competitiveness & Growth Programme
- https://www.gaisler.com/index.php/products/components/gr740
- Availability
  - Prototypes – available
  - Flight parts – contact sales@gaisler.com

# APPs GR740 board

## Software system – Overview

- RTEMS 5.1 used as the operating system for all GR740 applications
- Enables system to run in SMP and AMP mode
  - Simplifies integration with other applications running on unused CPU cores
- Management application performing APPs control and TM/TC routing executes on core 1
- Experiments running on the unused cores are booted into secondary applications
- Secondary application may start core 3 and 4 to run in SMP mode
- Applications linked with separate RTEMS kernels
- GRBOOT used as common bootloader
  - Code in MRAM can be READ by AMP applications

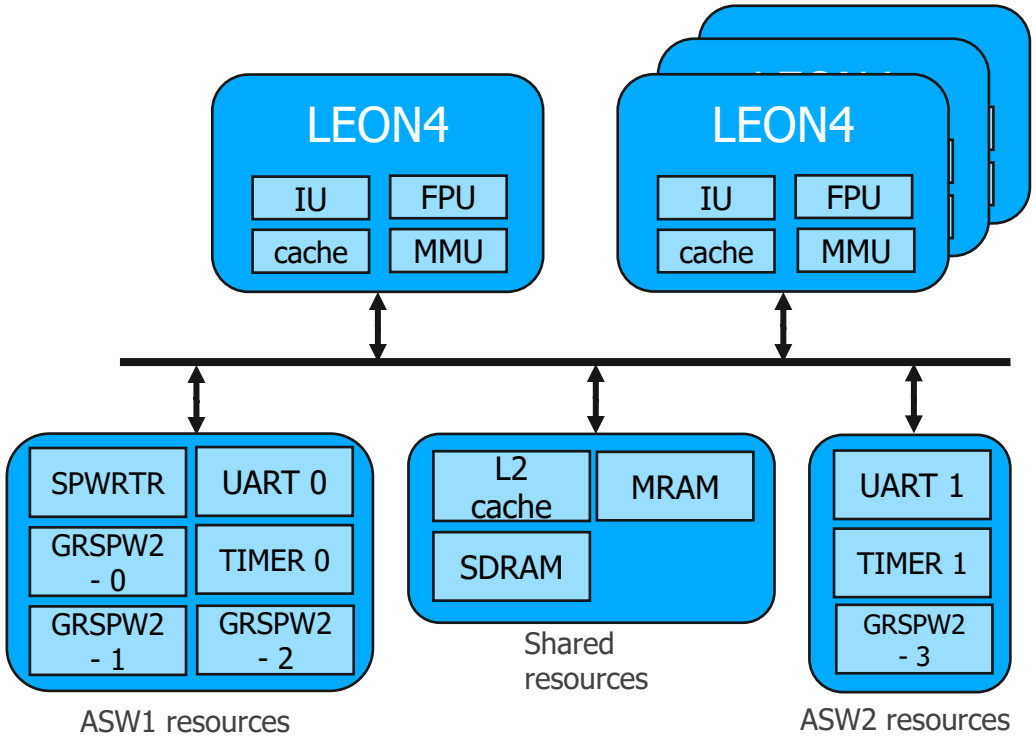


# APPs GR740 board

Software system – Multiprocessor configuration

## Multiprocessor execution

- SDRAM, L2 cache, and SpW router shared between applications
  - SpW router configured once. Secondary application does not interact with the router configuration registers.
  - RTEMS SpW driver allows both applications to be agnostic to which processor is using which GRSPW2 AMBA port and external interface
  - Memory management can be configured with MMU soft partitioning. Secondary application linked to memory offset 32MiB
  - No hypervisor or IOMMU
- Processor cores configured with MMU to protect memory between applications
  - 0x00000000 -> 0x02000000 used by core 1
  - 0x02000000 -> 0x20000000 used by core 2,3,4
- Device usage configured with the RTEMS driver manager
- Communication between primary application/OBC and secondary application performed via SpW router
  - Management application on core 1 can be agnostic to GNSS application running on cores 1 through 3
  - No shared memory OS directives required to pass data between applications



# APPs GR740 board

Software system – Multiprocessor configuration

**RTEMS driver manager configuration for second application**

```
/* Disable I/O cores which are not to be use but we include drivers for..
 * the cores we do not include drivers for will be ignored anyway
 *
 * Cores allowed:
 *
 *   - GPTIMER1
 *   - APBUART1
 *   - GRSPW3 (SpW Router AMBA Port3)
 *   - IRQMP[1]
 */
struct drvmgr_bus_res grlib_drv_resources =
{
  .next = NULL,
  .resource = {
    {DRIVER_AMBAPP_GAISLER_APBUART_ID, 0, NULL}, /* Do not use APBUART0 */
    {DRIVER_AMBAPP_GAISLER_GPTIMER_ID, 0, NULL}, /* Do not use GPTIMER0 */
    {DRIVER_AMBAPP_GAISLER_GPTIMER_ID, 2, NULL}, /* Do not use GPTIMER2 */
    {DRIVER_AMBAPP_GAISLER_GPTIMER_ID, 3, NULL}, /* Do not use GPTIMER3 */
    {DRIVER_AMBAPP_GAISLER_GPTIMER_ID, 4, NULL}, /* Do not use GPTIMER4 */
    {DRIVER_AMBAPP_GAISLER_SPW_ROUTER_ID, 0, NULL}, /* Do not use SpWRouter */
    {DRIVER_AMBAPP_GAISLER_GRSPW2_ID, 0, NULL}, /* Do not use AMBA Port0 */
    {DRIVER_AMBAPP_GAISLER_GRSPW2_ID, 1, NULL}, /* Do not use AMBA Port1 */
    {DRIVER_AMBAPP_GAISLER_GRSPW2_ID, 2, NULL}, /* Do not use AMBA Port2 */
    DRVMGR_RES_EMPTY
  }
};
#include <drvmgr/drvmgr_confdefs.h>
```

# APPs GR740 board

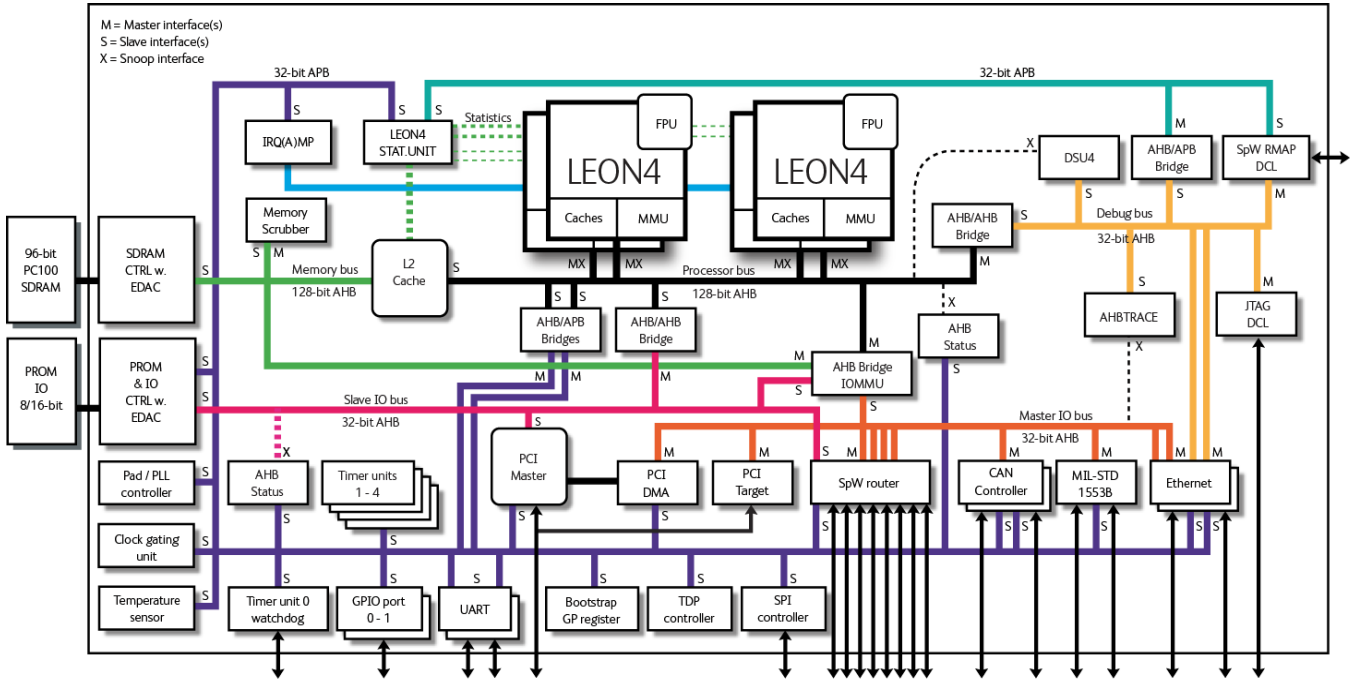
## Software system – FDIR operation

### SEU detection performed by primary application

- MEMSCRUB IP continually scrubs the SDRAM memory
- Built-in L2CACHE scrubber corrects L2 cache single bit/word errors
- L1 instruction and data cache periodically scrubbed
- MMU TLB periodically flushed
- IU and FPU registers periodically flushed
- SpW address buffers are automatically scrubbed by HW

### Actions required by secondary applications

- L1 instruction and data cache flush
- MMU TLB periodically flush
- IU and FPU registers periodically flush




### Fatal errors result in a controlled cold restart

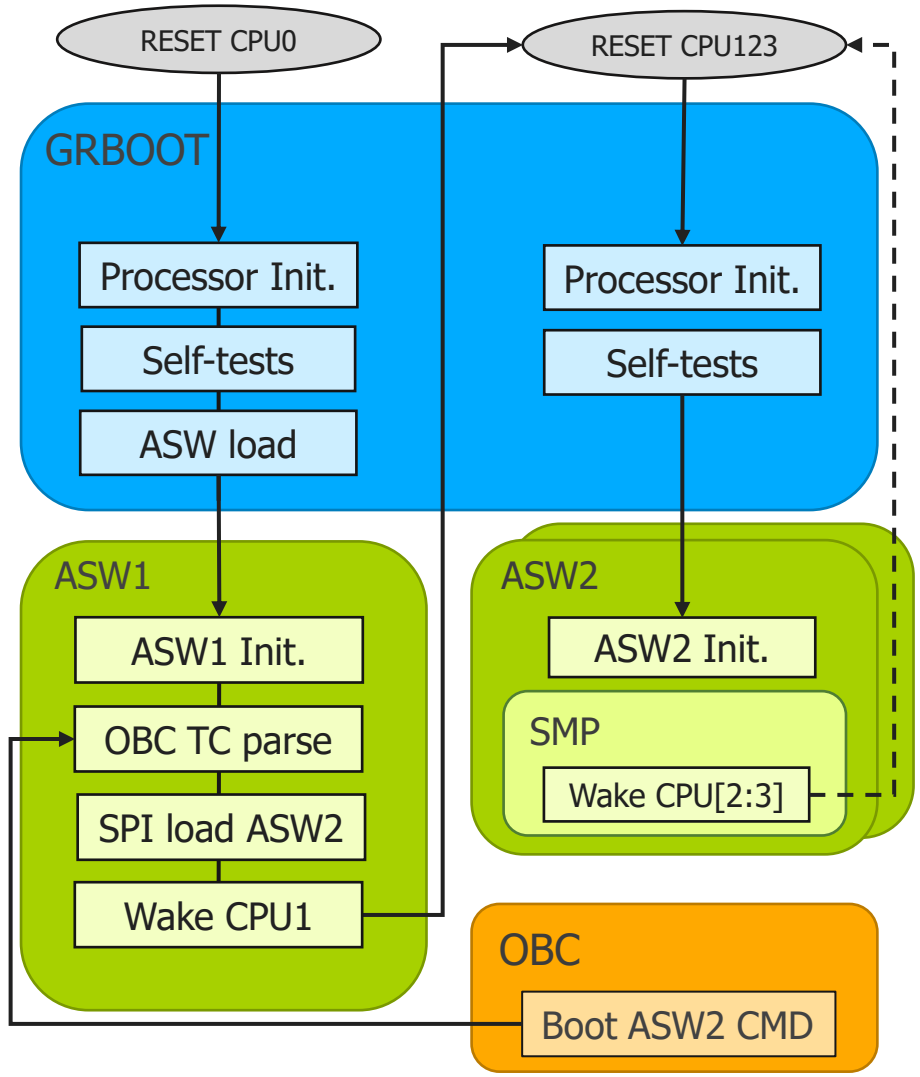
- Fatal error logged before shutdown
  - Downlinked after reboot for debugging when requested by GOMX-5 OBC
- If fatal error prevents SW execution, PLL Watchdog will reset board

# APPs GR740 board

Software system – Boot sequence

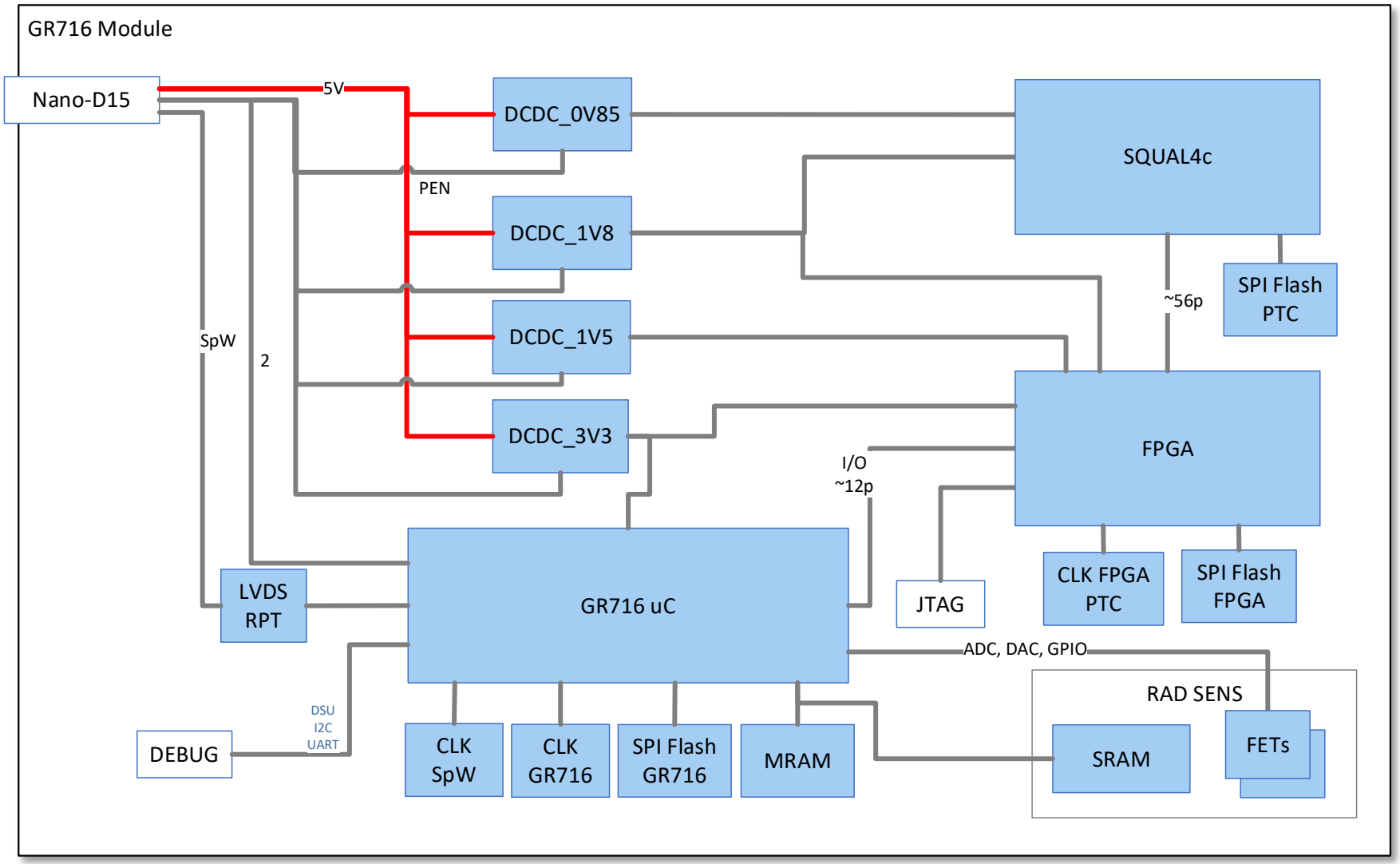
## GRBOOT used to fulfill APPs GR740 board requirements for system boot and bring-up

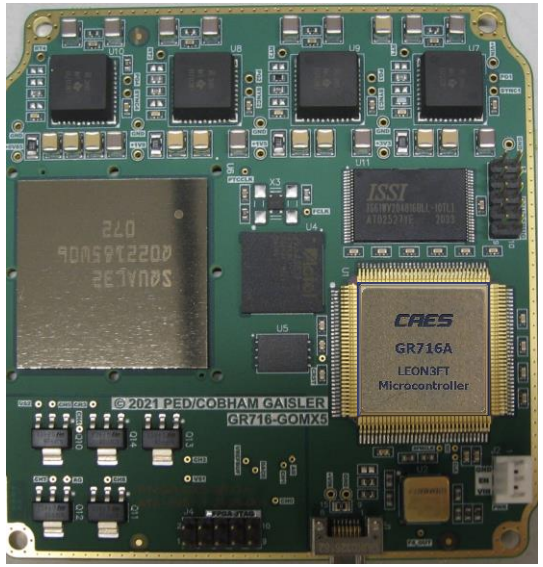
- Boot into management application on CPU core 1 (CPU0)
- On command from GOMX-5 OBC the ASW2 boot sequence begins on CPU1
- ASW2 can be Radiation experiment application or GNSS SDR experiment application
  - Radiation application
  - GNSS SDR application
- ASW2 never directly interacts with GRBOOT, telecommand is required to wake the application from ASW1
- ASW2 wakes CPU2 and CPU3 as required
  - CPU2 and CPU3 performs GRBOOT initialization unless ASW2 specifies the cores not to
- More information about GRBOOT itself will be provided in the afternoon

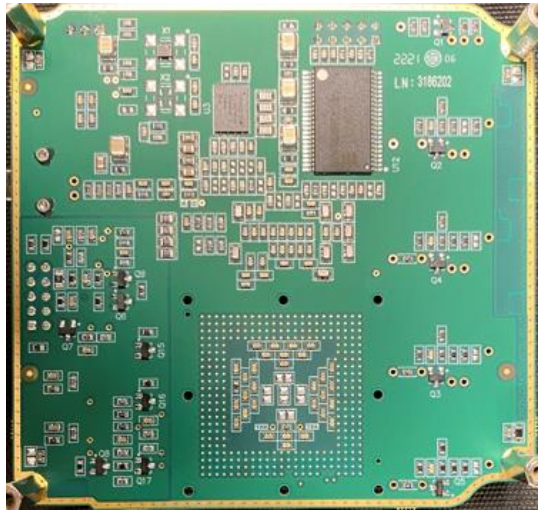


# APPs GR716 board interface

## Architecture



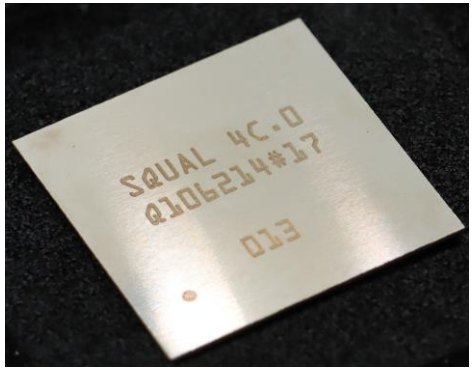



# APPs GR716 board

SQUAL4c component

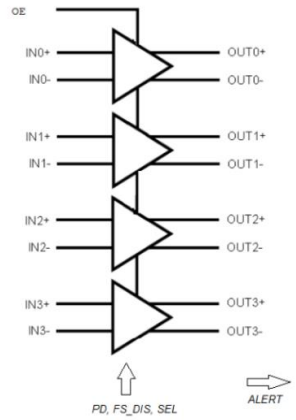
## SQUAL4c - LEON5/NOEL-V demonstrator

- Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor
- ST 28nm FDSOI GEO P2 technology
- Specialized design with LEON5 and NOEL-V sharing resources, consumes less than 1 $mm^2$
- Proves implementation on target technology
- Technology hardness and processor core fault tolerance features will be demonstrated through SEE test campaign
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain, fab in Crolles (FR)




## Quad LVDS Buffer/Repeater

- Part no GR54LVDS054PZ
- Dedicated design for SpaceWire interfacing
- 25-pad ceramic land grid array package
- Radiation hard >300 krad (Si), SEL and SEE immune
- Up to 400 Mbps switching rates



# APPs GR716 board

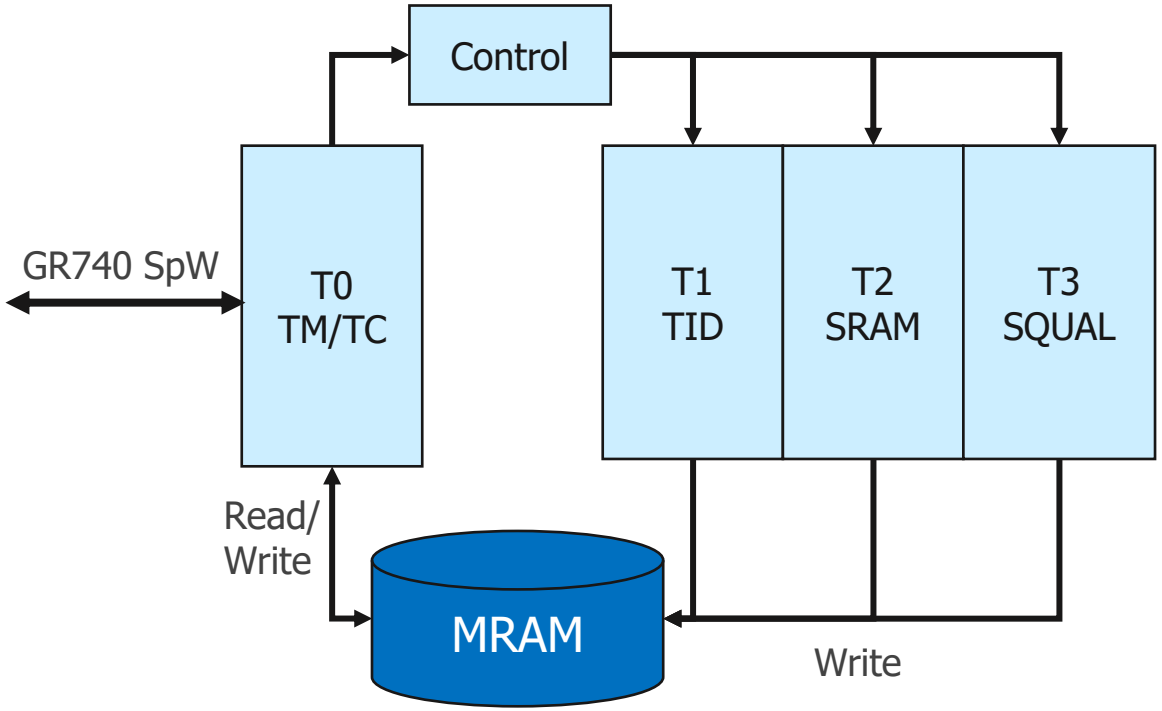
Software system

## Operating system

- Zephyr RTOS Version 2.5.0
- GR716A BSP used supporting:
  - Interrupt controller
  - UART
  - Timer
  - GPIO
  - ADC
- BCC Drivers used for SpW
- ASW updates provided via RMAP by GR740

## Low power mode

- Power to SQUAL4 part of board disabled by GR740
- SpW ports clock-gated off
- SpW transciver disabled
- T1 TID experiment continue in this mode
- GPIO from GR740 used as wakeup signal



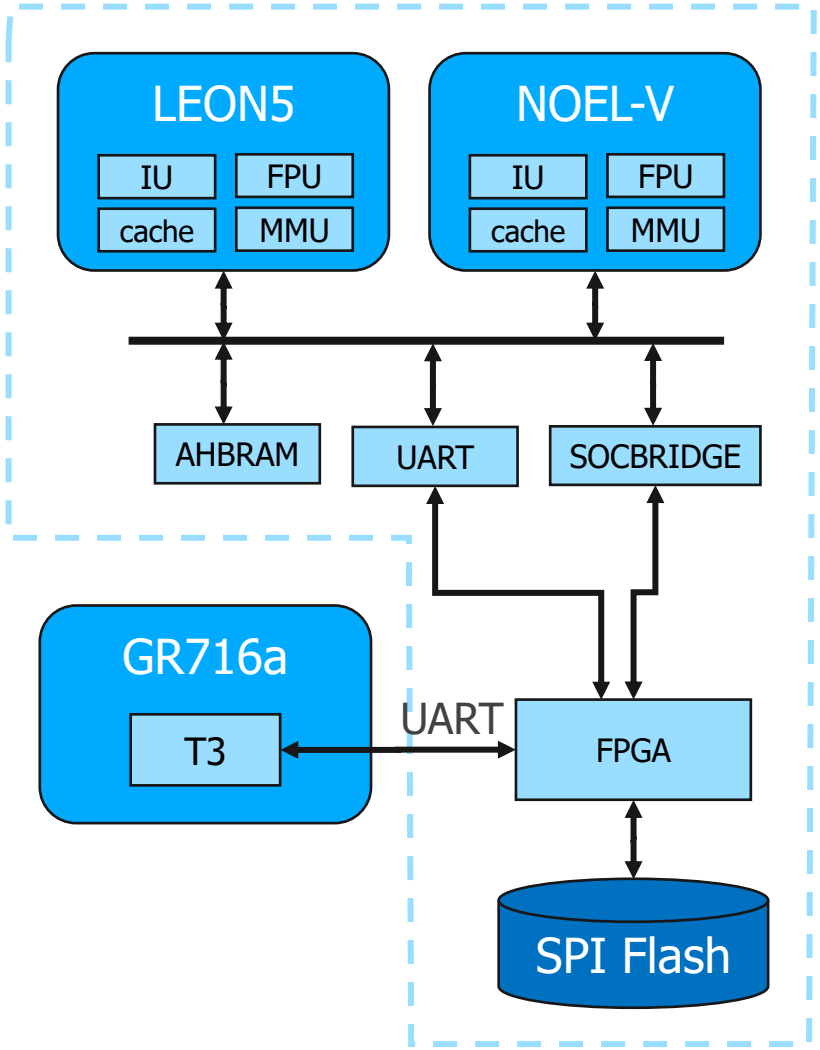

Zephyr™ Project

# APPs GR716 board

Software system – SQUAL4c interfaces

## SQUAL4c features

- Executes LEON5 or NOEL-V core if SQUAL4c circuit enabled by GR740
- Performs EDAC monitoring of internal caches and AHBRAM
- EDAC events reported to GR716 via UART
- Test progress is reported to GR716 via UART to indicate alive status
- Shared Application code in FPGA SPI Flash
  - FPGA acts as SPIM controller
  - FPGA performs address translation based on which CPU core is booting
  - Separate area in SPI flash used to store each cores application code



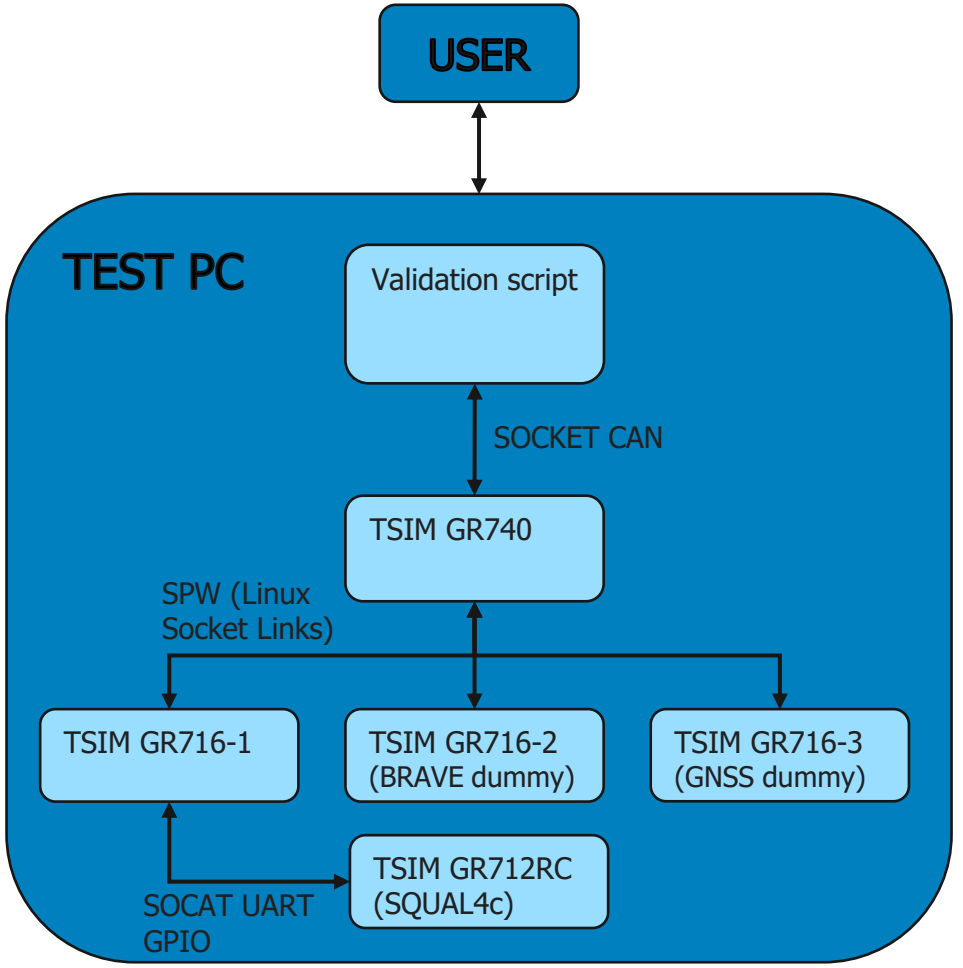

*SQUAL4 board section*

# Development and Validation setup

## Simulator environment

**Simulator environment created to support development and validation efforts**

- TSIM used to simulate GOMX5-APPs Gaisler boards
  - GR740, GR716 and "SQUAL4c"
- HW CAN interface emulated with Socket CAN
- SPW packets between TSIM instances sent as IP packets via linux socket interfaces
  - Extra dummy GR716 TSIM instances used to "simulate" BRAVE and GNSS TM/TC traffic
- UART connection between GR716 and SQUAL4c performed using Socat interface
- SQUAL4c software simulated in a GR712RC TSIM environment
  - Purpose is to test UART interface
- Time synchronized to actual time for time critical validation tests

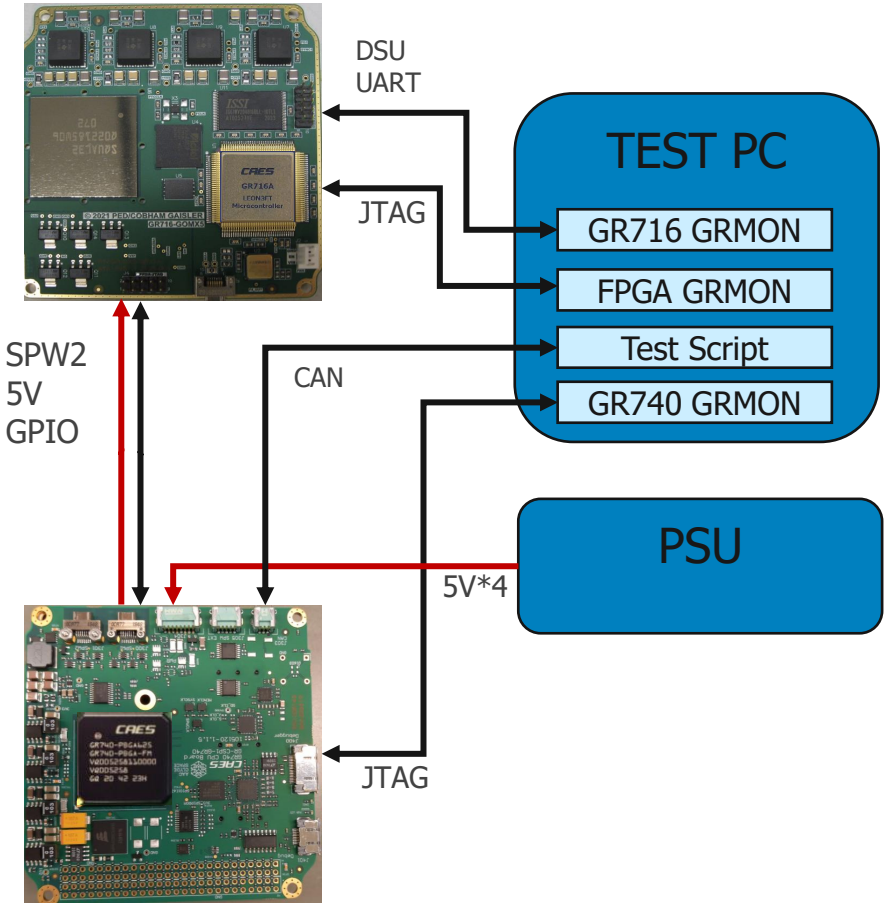


# Development and Validation setup

Hardware environment with EM boards

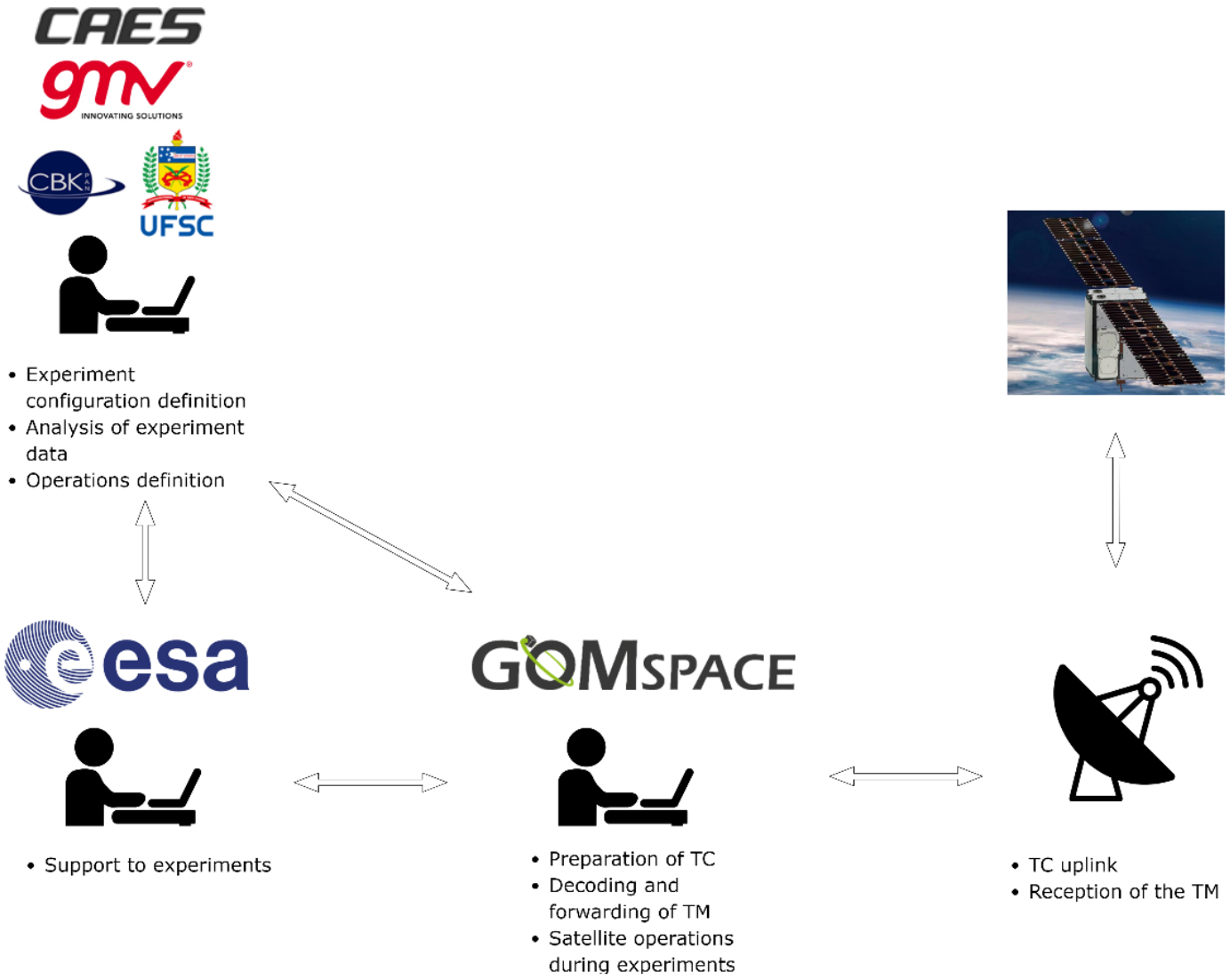
## EM board HW Validation setup

- PCAN USB used to send CSP CAN frames between test PC and GR740
- JTAG interface used with GRMON to flash GRBOOT and ASW to MRAM to GR740
  - Subsequent use of JTAG is mainly for development and debugging purposes
- Initial program supplied to GR716 since RMAP is not enabled by default
  - Application updates can then be provided using SPW RMAP
- GRMON connected to SQUAL4c via the FPGA SOCBRIDGE on GR716 board



# Objectives and experiments

## Experiments operational flow



# Objectives and experiments

Subset of experiments

| # | ID | Experiment | Scope | Prel. duration |
|---|---|---|---|---|
| 1 | APP-01 | Gaisler multi-experiment | Perform all sub-experiments/applications on the GR740 and GR716 boards. Includes TMC, housekeeping, memory scrubbing, SQUAL4c demonstration and SEU detection on multiple chips. | Sequences spread out over mission |
| 2 | APP-01LD | Gaisler - long duration | Long duration radiation experiments. SEU on CERN SRAM and TID measured. (The devices must be biased all the time when subject to radiation, for correct data). | Full mission duration |
| 3 | GNSS-SW1 | GNSSW mono frequency receiver on GR740 | The experiment focuses on testing the mono frequency (E1/L1) receiver running on LEON4 processor with different SW configurations. | A few days |
| 4 | GNSS-SW4 | GNSSW mono frequency receiver on GR740 with Brave as samples distributor | The experiment focuses on testing the single frequency (E1/L1) receiver running on GR740 processor with Brave board as samples distributor. BRAVE will also host a hardware FFT-based GNSS fast acquisition unit. | A few days |

# Test campaign

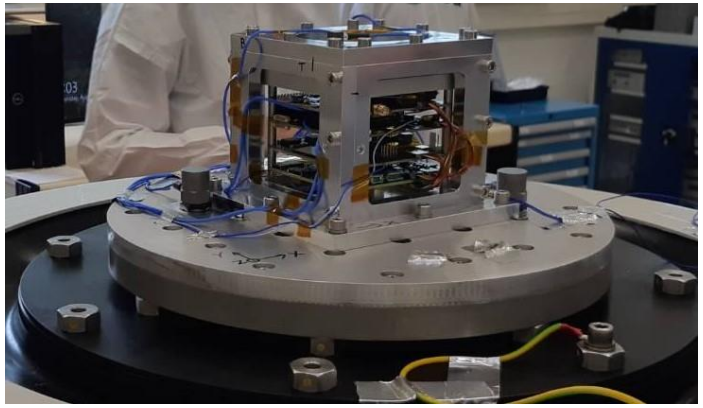
Overview

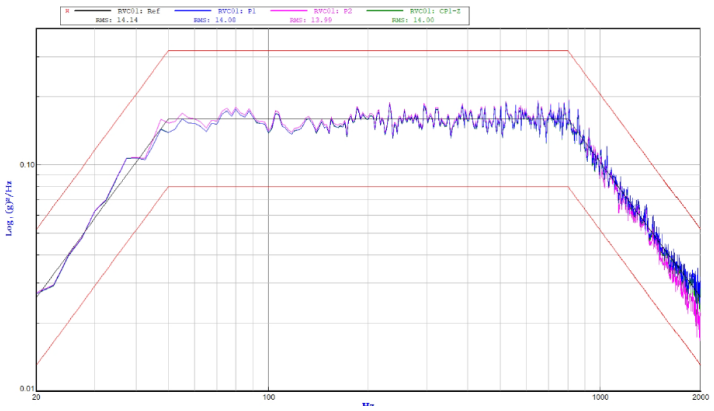
- Functional and Performance Tests
  - EM boards
  - Locally at each partner
- APPs Integration Tests
  - EM boards
  - Mostly at Gaisler
  - Mostly done, some remain
- Environmental Tests
  - Qualification Levels on EQM boards
  - At ESTEC as joint ESA-APPs
  - teamwork
  - First phase done
- S/C Integration Tests
  - EM boards
  - At GomSpace
  - On-going, initial phase started
- Mechanical Tests
  - Acceptance Levels on FM boards
  - In planning phase

# Test campaign

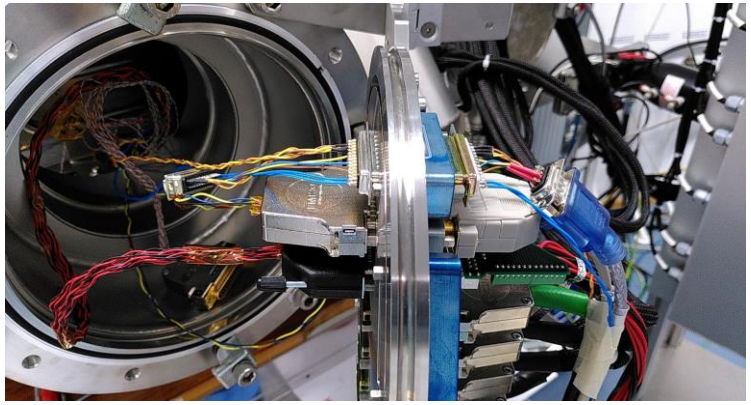
## Environmental Tests on EQM stack

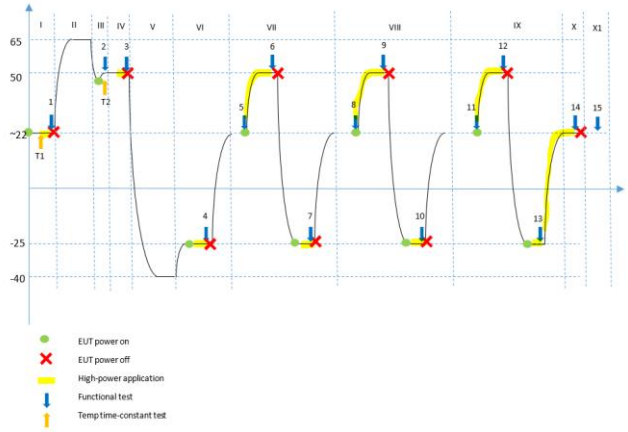
### Vibration



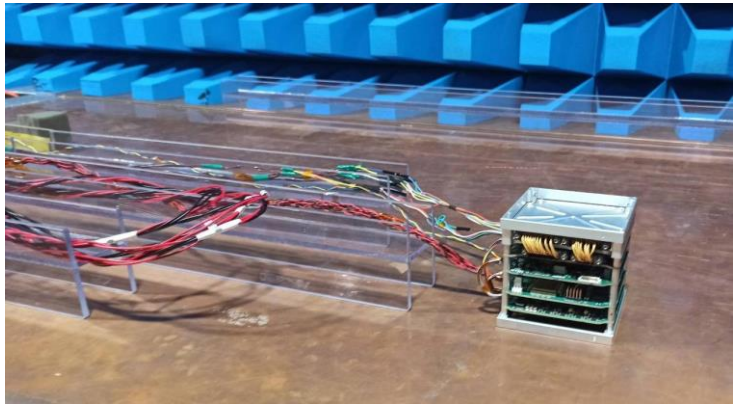


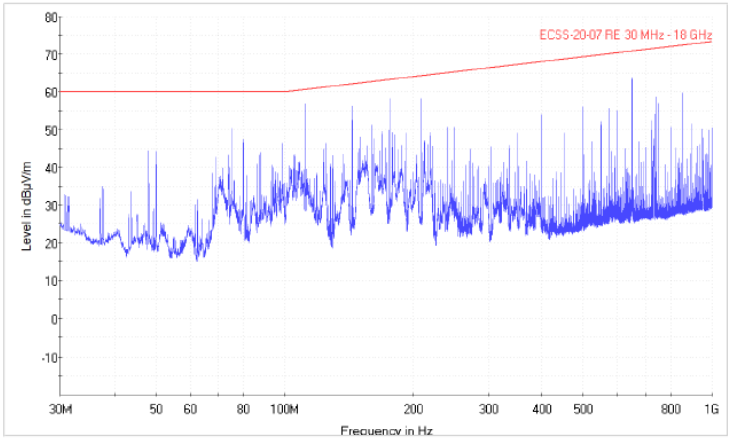
### Thermal vacuum






### EMC

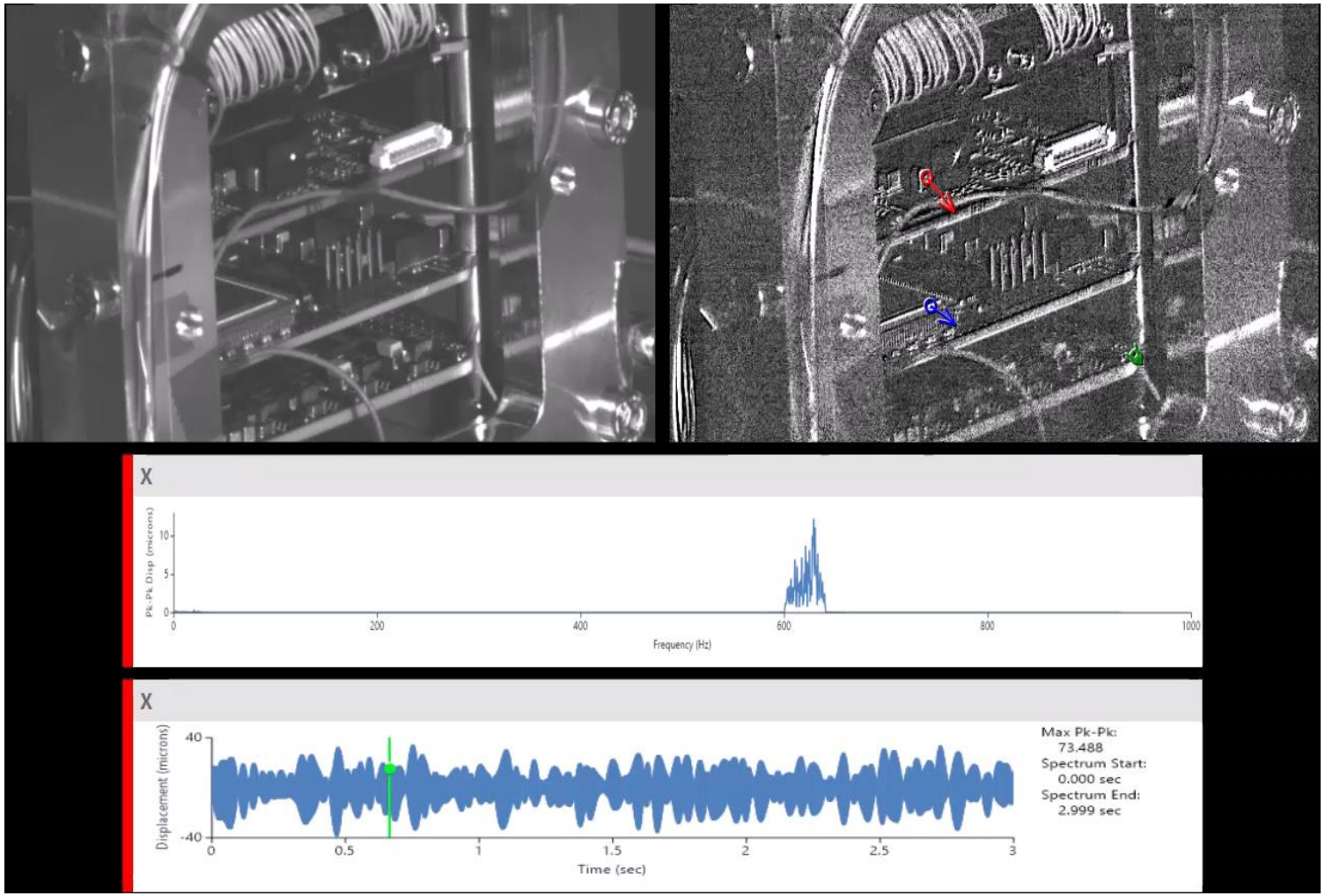




# Test campaign

## Vibration tests issues

- GEVS profile used
- Initial vibration tests used accelerometers
- High speed camera used during vibration analysis to compare against accelerometer values
- New vibration tests planned for 2023 with reinforced boards and frame



# Conclusion

- The GOMX-5 APPs module has been developed, based on new concepts, components or variants.
- Simulator test environment provided for more efficient integration of GR740 and GR716 into the APPs payload.
- Tests have been performed on EM and EQM boards.
- Further iterations of mechanics is ongoing, including a follow-up test campaign.
- Preparation of Flight Model (FM) variants of the boards is on-going with various progress.

# For further information and inquiries

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- Thank you for listening!


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