EMBEDDING INNOVATIONS





PIKEOS FOR GR740 IN SPACE RIDER

Thierry Maudire, Dec 2022

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PRESENTER





Thierry Maudire Head of Technical Sales

- Management and coordination of Solution Architects team to address customers technical requirements in different industries such as Aerospace & Defense, Automotive, Railway, and Industrial.
- About 30 years of experience specifying and developing solutions for embedded systems. Prior to SYSGO, he held different positions at Wind River Systems Inc.
- Education:
 - Postgraduate Degree, in Robotics, from University Pierre et Marie Curie (Paris)
 - Master of Sciences in Signal Processing and Telecommunication from University of RENNES

ABOUT SYSGO



- Leading European OS vendor for embedded systems.
- +30 years certification experience of Safety-critical systems.
- Products:
 - PikeOS certifiable hard RTOS + Type 1 Hypervisor
 - PikeOS for MPU
 - ELinOS embedded Linux Distribution
- PikeOS supports the highest Safety and Security standards, like ECSS Cat. A and CC EAL5+.
- BSPs, certification kits and consulting services.
- Part of the Thales Group.







EMBEDDED PERFORMANCE FOR CRITICAL SYSTEMS



• PikeOS

Certified hard real-time OS (separation kernel with type-1 hypervisor)

• PikeOS for MPU

- Certified hard real-time OS for MPU processor
- ELinOS
 - Embedded Linux distribution
- CODEO
 - Integrated Development Environment based on Eclipse
- Field proven
 - Avionics, Automotive, Defense, Industrial, Medical, Railway and Space applications

Seamless customer product development and

management:

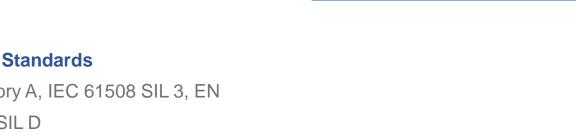
- System architecture and Security approach
- Hardware integration
- Long term customer support
- Tools and services to cover the full product life cycle



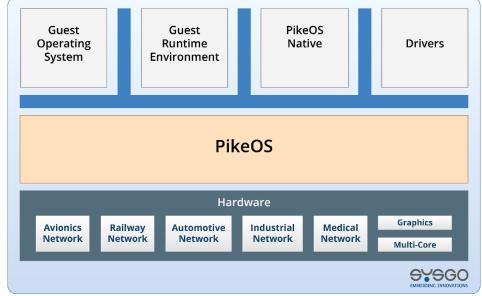
PRODUCTS & SERVICES PIKEOS - EMBEDDED RTOS & HYPERVISOR



- Hard Real-Time Operating System and Hypervisor
- Guest operating systems
 - Linux, POSIX, ARINC-653, AUTOSAR
- Wide range of CPU supported
 - PowerPC, ARM, x86, LEON3 & 4, RISC-V
- Mixed criticality
- Without any export restriction
- Common Criteria EAL 5+ certified* Separation
 - **Kernel Architecture**
 - Certifiable to the strictest Safety Standards
 - DO178C DAL A, ECSS Category A, IEC 61508 SIL 3, EN 50128 SIL 4 and ISO 26262 ASIL D
 - Multi-Core certification





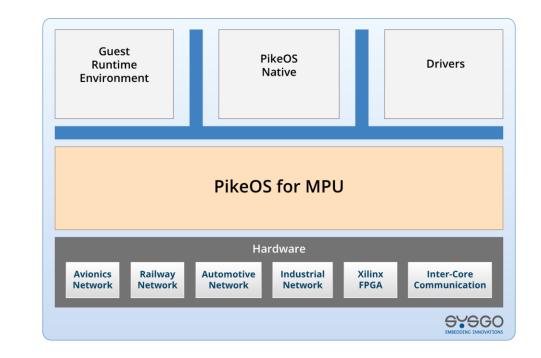




PRODUCTS & SERVICES PIKEOS FOR MPU



- Re-use for PikeOS and adapt for MPU processors
- RTOS and separation kernel-based hard real-time operating system
 - Robust time & resource partitioning
 - AMP multi-core processor support
 - Hardware abstraction
 - First level exception and interrupt processing
 - Thread management & scheduling
 - Health monitoring
 - Inter-partition communication and synchronisation
 - ICCOM (Inter-Core Communication)
 - I/O device abstraction and access control
- CODEO, Eclipse-based IDE
- PikeOS compatibility
- Large software & hardware eco system
- First implementation in Space on DAHLIA
 NG_ULTRA SoC in Space Inspire





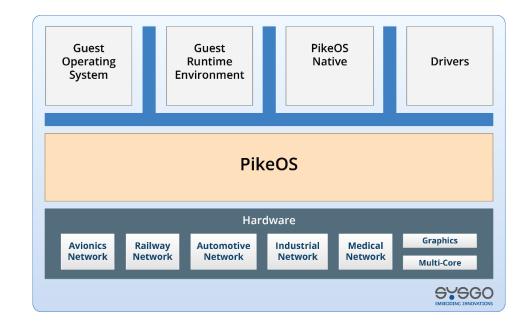
PRODUCTS & SERVICES PIKEOS AND GR740



- ASP (Architecture Support Package)
 - SPARC LEON4
- PSP (Platform Support Package)
 - Compatible with GR740 and TSIM (v3)
- Drivers
 - Ethernet, Serial
 - Additional drivers being developed by Thales Alenia Space

• Add-ons

- Dynamic Ticker
- IOMMU Support
- Configurable Reset Mode
- MAF Synchronization on external event
- Overrun Management



PRODUCTS & SERVICES CERTIFICATION



Safety

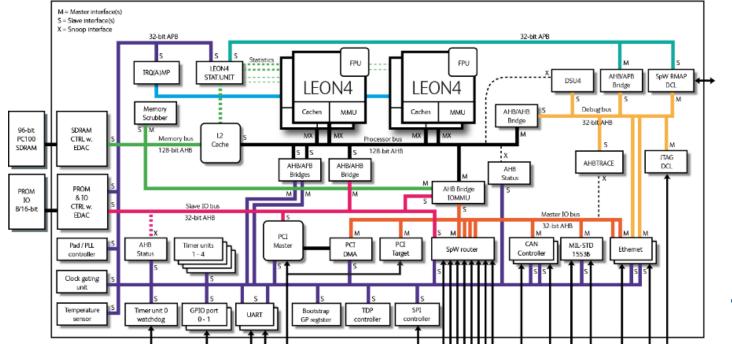
- Target : ECSS Category A
- Approach
 - Re-use existing experience and knowledge from Avionics Multicore DO178C/AMC 20-193 standard and outcome of ESA contract No.4000125316/18/NL/AF with a mapping between Avionics and Space Safety standards
 - Source/Object Code Traceability : ESA approach in document Prepared by Thanassis Tsiodras TEC-SWE Reference TEC-SWE/17-945/TT
- Rerun test suites on TAS hardware
- ISVV Kit
 - Ready to deliver PC with Qualification Data
 Package, source code access and consulting
 hours
- ESA participation to Reviews

• Cyber Security

- Based on PikeOS 5.1.3 separation kernel with CC EAL5+
 - CC Certificate for x86, ARMv8, PPC could be extended to incorporate SPARC LEON4 ASP
- ITT CYBERSECURITY BY DESIGN FOR MIXED
 CRITICALITY EMBEDDED SYSTEMS
 - On-going activity on PikeOS for MPU for Cortex R52 (ARMv8-R) architceture

RETEX ON GR740 EXPERIENCE





• Pros

• Well defined architecture:

Cache coherency between cores,

IOMMU, DRAM Scrubbing in HW

- Improve performance compared to LEON 3, while still retaining IPs (IO)
- GRMON debugger, PikeOS integration in GRMON (in progress)
- Simulation environment via TSIM
- Cons
 - Unique Processor memory bus could generate bottleneck
 - No last level cache partitioning in HW

TOOLING GRMON PIKEOS AWARENESS INTEGRATION

- Prototyping activity done by Gaisler with SYSGO Support
- Visibility of PikeOS threads/tasks, etc
- Stack Backtrace of executing and switched out threads
- Support demonstrated on GR740/PikeOS-5.1
- Work in progress but should be available with one of next GRMON version
- Work being done also on NOEL-V 32/64-bit

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+ SpExisting session	Name	Туре	Value			-11-0	Нех		Description Addres	
🕶 🔁 GR740 rev0	▼ ♦ psp	P4 psp descripto	{api versions	-9xf8f89800, max interrupts=		Phile D			restato registers	
🕨 🧬 cpu0 (Power down mode)	00-api version	P4 uint32 t	9xf8f80300			pcitrace0			pcitrace0 registers	
P cpu1 (Power down mode)	op max interr	P4 uint32 t	0180866360			uart0			uart0 registers	
P cpu2 (Power down mode)	66-ts calibrati	P4 uint64 t	0+00000300300	0.05100		 status 	80008855		UART Status registe .0xFF900	
🕨 🧬 cpu3 (Power down mode)	terns per cal	Mitimeit	9x898d5100306	366038		ctrl	88008803		UMRT Cantrol registe 0xFF900	
* 🔐 Pike05	the dyntick re-	s P4 time t	9+893+99999101	76c98		scaler	00000032		UART Scaler register ExFF906	0030
🕨 🧬 Switcher#00 (Suspended)		z P4 time t	0xc4830300340	064001		uart1			uart1 registers	
🕶 🧬 idleA00 [cpu0] (Power down mode)	P = psp.id	const char *				10:00			gpio0 registers	
0x83022e88 in psp_idle_workaround() at libpsp/lean-power-down		const char *				iodata	88063311		I/O port data registe 0xFF902	
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0x8202764c in enter_idle() at src/main.c: 1392	er align mask	P4 address t	0xc4Z3ed14			iremask	88006830		1/0 interrupt mask r 0xFF902	
 0x81028e24 in p4 main() at src/main.c: 1240 	► 🚍 aqi	P4 gsp api t		0001. init_cpu=0x22228000, i	nit 1	ingpol	0000b45d		UO interrupt polarity 0xFF902	
0x810233cc in init_beard() at src/cbost.c: 245	▶ @ arch	P4 psp arch t		c+0x00bg2010, ram phys size	09100	rgedge	88003ecf		1/0 interrupt edge r 0xFF902	
0x010001000	MP break on	adt beoi t	-1341128512			▼ capability	99056491		Capability register 0xFF902	
0x0100010x0	M PUT CPU	P4 uint12 t	0+b08e28ff			28 pu			Pulse register availa 0xFF903	
ts (3 n 0000000 in R) at	8x808d51683066800					17 ier			Input enable registe 0xFF902	
🕨 🧬 Switcher#01. (Suspended)	Hext 800451068006 Bloc 1058, 0583, 061	4800, Dec: 922712027 80 1101 6101 8001 0	4141741056. Oct: 0	1000152420026001400000 8,6000,0110,0000,0000,0000,0000		26 1f			Interrupt flag regist ExFF902	
🕶 🧬 idle#01 (cpu1) (Power down mode)	Size: Shytes, Type	Size: 8 hytes, Type: P4 time t					84		Interrupt generation 0xFF903	
Ox82022e88 in psp_idle_workaround() at Ibpsp/een-power-down	c: 54 Offset: 15. Addres	m: 0x80064014				4:0 nl:	. 0f	15	Number of pins in C 0xFF902	201C
0x830284dc in p4_idle[] at src(main.c: 1719	By Disassembly 22	# Terminal					- 0	K Expressions 22		
Ox830501d0 in p4sparc_enter_idle() at arch/sparcisrc/acentext.5		a								
Ox8202794c in enter_idle() at src/main.c: 1392				Ente	r location he	ne 👻 🌒	1a 😫 🔍	😓 🍕 🖃	◆ × 後 € □ ゼ	4
Switcher#02 (Suspended)	83628df4; 0	no 501, 6		<pre>sp4_main+1856></pre>				Name	Туре	
Idle#02 [cpu2] (Power down mode)		ne.a 6x88028e2c		sp4 main+1860>				v Catolic	P4 taskdesc t [256]	
🕨 🎤 Switcher#03 (Suspended)		ethi %hi(0x80059	090), ho6	<p4_main+1864></p4_main+1864>				w 10.991		
Idle#03 [cpu3] (Power down mode)		all 0x80038990		<p4_main+1868> <p4_main+1872></p4_main+1872></p4_main+1868>				(0)	P4 taskdesc t	
🕨 🧬 Sysgo (Suspended)		ep ev 0x20, %o2		<p4_main+1872> <p4_main+1875></p4_main+1875></p4_main+1872>					P4 taskdosc t	
🕨 🧬 log_hmev (Suspended)		eth1 3h1(0x80055	030), 501	-sp4 main+1880>				* * td	P4k taskinfa t *	
🕨 🧬 service (Suspended)		r %01, 8x3e8, %c	1	<p4_main+1884></p4_main+1884>				MP taskno	PM tank t	
# Pfirst_partition (Suspended)		all 0x800252d0		<p4 main+1888=""> <p4 main+1892=""></p4></p4>				of is termin	natin P4 uint8 t	
second_partition (Suspended)		dd %s0, 0x130, % all 0x80627cd4	101	<p4_main+1892> <p4_main+1896></p4_main+1896></p4_main+1892>				Ob- sinused	5 P4 uint8 t	
🕨 📌 ieon3-uart (Suspended)		ev 0. tot		<pre>spin=1900></pre>				OP unused	6 P4 unt6 t	
🕨 🧬 fop_0_0 (Suspended)		all 0x80027f34		<p4_main+1904></p4_main+1904>				04 unused	7 P4 uint8 t	
fop_0_1 (Suspended)		ov 0, hot		<p4_main+1908></p4_main+1908>				respect	struct P4k respart str	× *
#fop_0_2 (Suspended)		all 0x8083a398 r 308.0x238.3x		<p4 main+1912=""> <p4 main+1916=""></p4></p4>				+ + parent	struct P4k taskinfo st	
Image: Prop. 0 _3 (Suspended)		r 108, 98238, 10 ev 9, 102	~	<p4_main+1920> <p4_main+1920></p4_main+1920></p4_main+1920>				0x08000601		
fop_0_4 (Suspended)	83628c38: a	dd Nfp, -4, Nol		<p4_main+1924></p4_main+1924>				Hex: 00600061, Dec: 1, O Bin: 0602,6000,8000,800		
§ P 5Y5_irq_29 (Suspended)		all 0x800358e4		<p4_main+1928></p4_main+1928>				Size: 4 bytes, Type: P4 t	ssk.t	
Fys_irg_30 (Suspended)		ov 0, hoB		<p4_main+1932></p4_main+1932>				Offset: 0. Address: 6x80	00000	
# Pfirst_process (Suspended)	83628e44: 0	np %s0, 8		<p4_main+1936></p4_main+1936>						
E hoead 123456 (Suspended)										



THALES ALENIA SPACE USE CASE: TAS OBC – GR740 BASED

ESA Projects

- Main OBC of the satellite for orbit control, ground communication...for
- Galileo
- Copernicus
 - CHIME
 - CIMR
 - ROSE-L
- Space Rider
- Italian Confidential Project







SPACE RIDER

- **Uncrewed Robotic Laboratory** will stay in low orbit for about two months.
- At the end of its mission, Space Rider will return to Earth with its payloads and land on a runway to be unloaded and refurbished for another flight.
 - ESA signed in December 2020 a contract for delivery of the Space Rider _ flight model including the reentry module and the AVUM orbital service module, by co-prime contractors: Thales Alenia Space Italy and Avio S.p.A.
 - In addition, other subcontractor GMV is also involved and using PikeOS _
 - TAS main **On Board Computer** manages all the spacecraft and is _ responsible for its safety behavior
 - ECSS Cat. A is mandatory because the spacecraft will return to earth and share the sky with civilian airplane









QUESTIONS OR COMMENTS?

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SYSGO GmbH

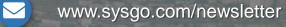
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