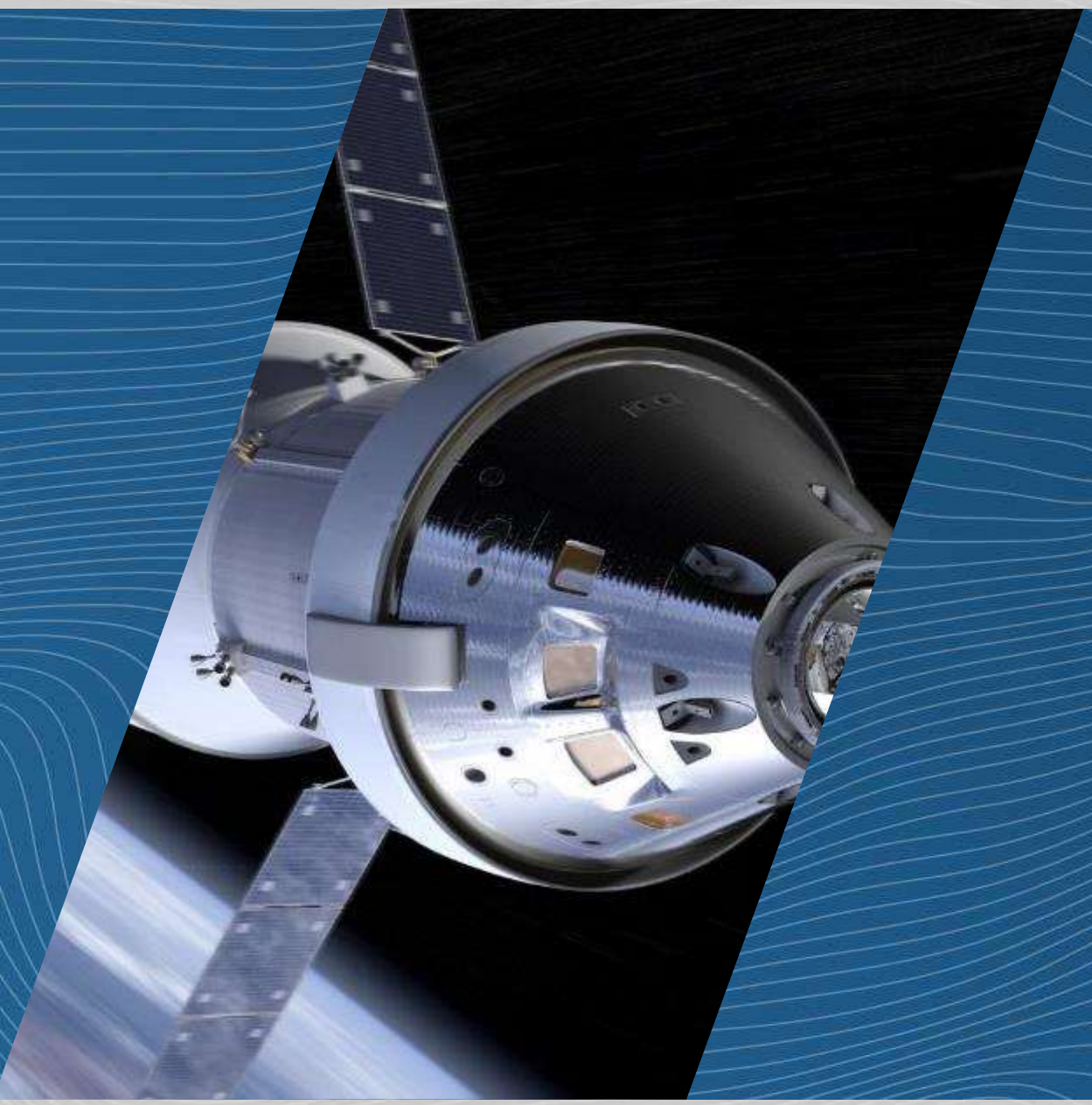

CAES PIONEERING ADVANCED ELECTRONICS

GR765 Development Status

GR740 USER DAY | 2022

13th of December 2022

ERASMUS Auditorium, ESTEC

Fabio Malatesta

2022-Dec-13

GR740 - Quad-Core LEON4FT Processor

CAES PIONEERING ADVANCED ELECTRONICS

Value proposition

- High performance, wide range of interfaces
- SPARC V8 compliant, Radiation-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- Low risk, off-the-shelf product, QML Q/V
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS (1000 MIPS)

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/LandandMaritime		
	CHECKED BY Phu H. Nguyen			
	APPROVED BY Muhammad A. Akbar	MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 22-04-18			
	REVISION LEVEL	SIZE A	CAGE CODE 67268	**5962-21204**
		SHEET	1 OF 51	

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esa LEON SPARC Compliant SCD V8

GR740 - Quad-Core LEON4FT Processor

CAES PIONEERING ADVANCED ELECTRONICS

What can be improved?

- Less pin muxing
- Costumers require:
  - Higher performance memory interface (DDR3/4)
  - NAND memory controller for storage
  - High Speed Serial Links Controllers
- Software vendors outside of space industry do not target SPARC
- A SBC based on the GR740 typically requires a companion FPGA

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Phu H. Nguyen CHECKED BY Phu H. Nguyen APPROVED BY Muhammad A. Akbar DRAWING APPROVAL DATE 22-04-18 REVISION LEVEL	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/LandandMaritime MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON SIZE A / CAGE CODE 67268 / **5962-21204** SHEET 1 OF 51

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GR765

Next-Generation SoC

GR765 – Overview

- **Phase 1A (funded): DARE65 Demonstrator** – Downsized implementation of GR765 architecture. Availability TBD for eval board with plastic parts in 2023.
- **Phase 1B/2A/B (funded): GR765-XX** – GR765 implementation. Goal is 2024 component availability. Projects started.
- **Phase 3A/B: GR765-CP/MP/MS** – GR765 product (same design as GR765-XX) with Qualification & production flows/temperature ranges available as per other CAES standard products. Availability (flight models) is TBD.
- **Phase C: GR765-*-C(C/L)GA** – Ceramic package development
- **Complemented by:** ESA Fifth Generation Space Microprocessor development

GR765 is a new component development based on an extended GR740 SoC design

The development of the demonstrator and the updates of the SoC design to form the GR765 are undertaken in ESA GSTP, ARTES Competitiveness & Growth, and NAVISP EL2 activities with funding from the Swedish National Space Agency and CAES.

Disclaimers:

GR765 Effort is on-going & subject to change without notice. Currently there is no guarantee of a product launch.

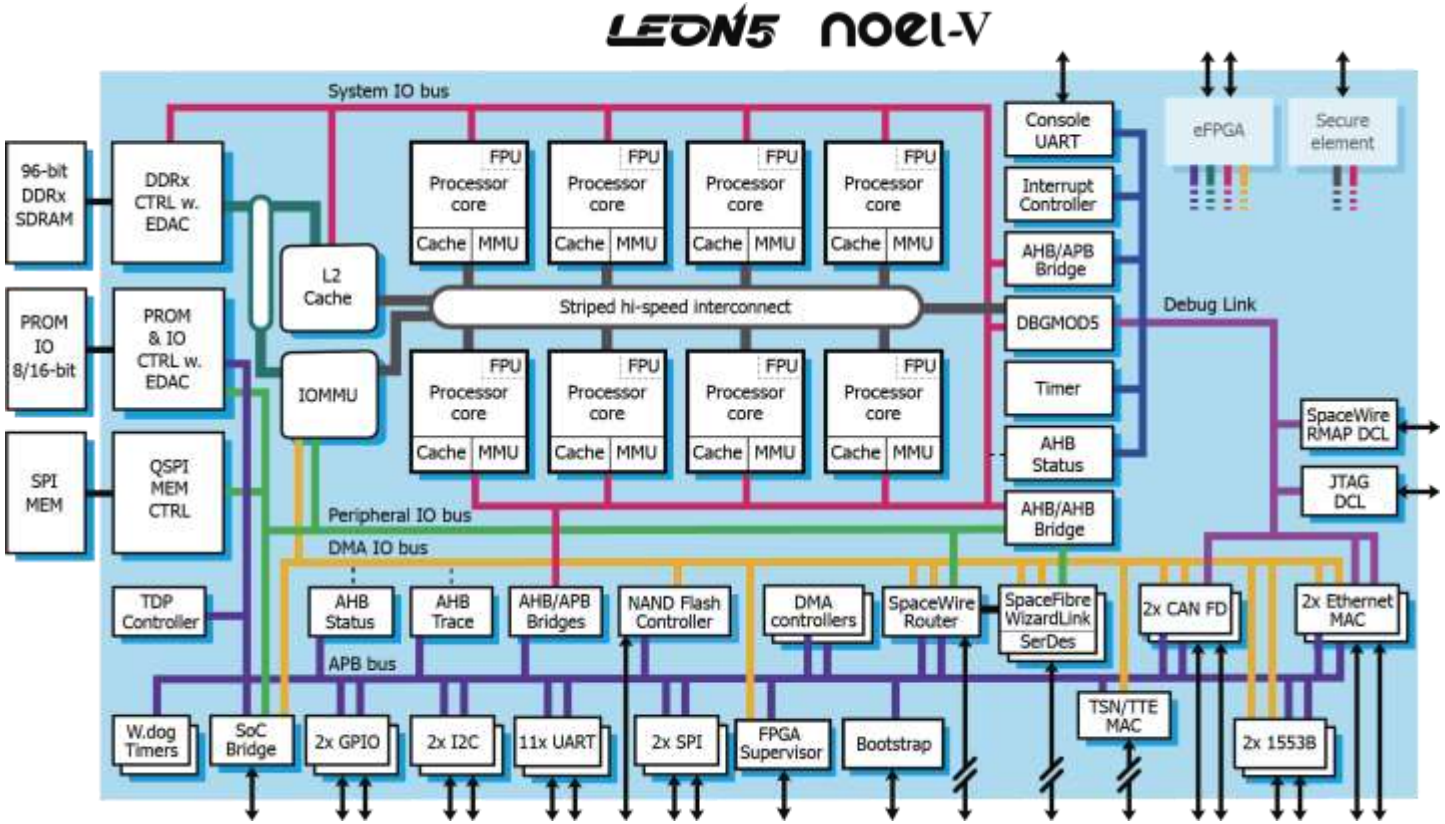
Contact Gaisler to receive the latest available information.

GR765 – Octa-Core Processor

In development
No guarantee of product launch

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **Target technology: STM 28nm FDSOI**
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR3 interface with dual x8 device correction capability**
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **Secure Element, providing Secure (authenticated) boot (TBD)**
- **eFPGA ~30k LUT (TBD)**
- **High-pin count – LGA1752 package allows reduction of pin sharing**



SPARC RISC-V®

Instruction Set Architectures

Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

Why SPARC?

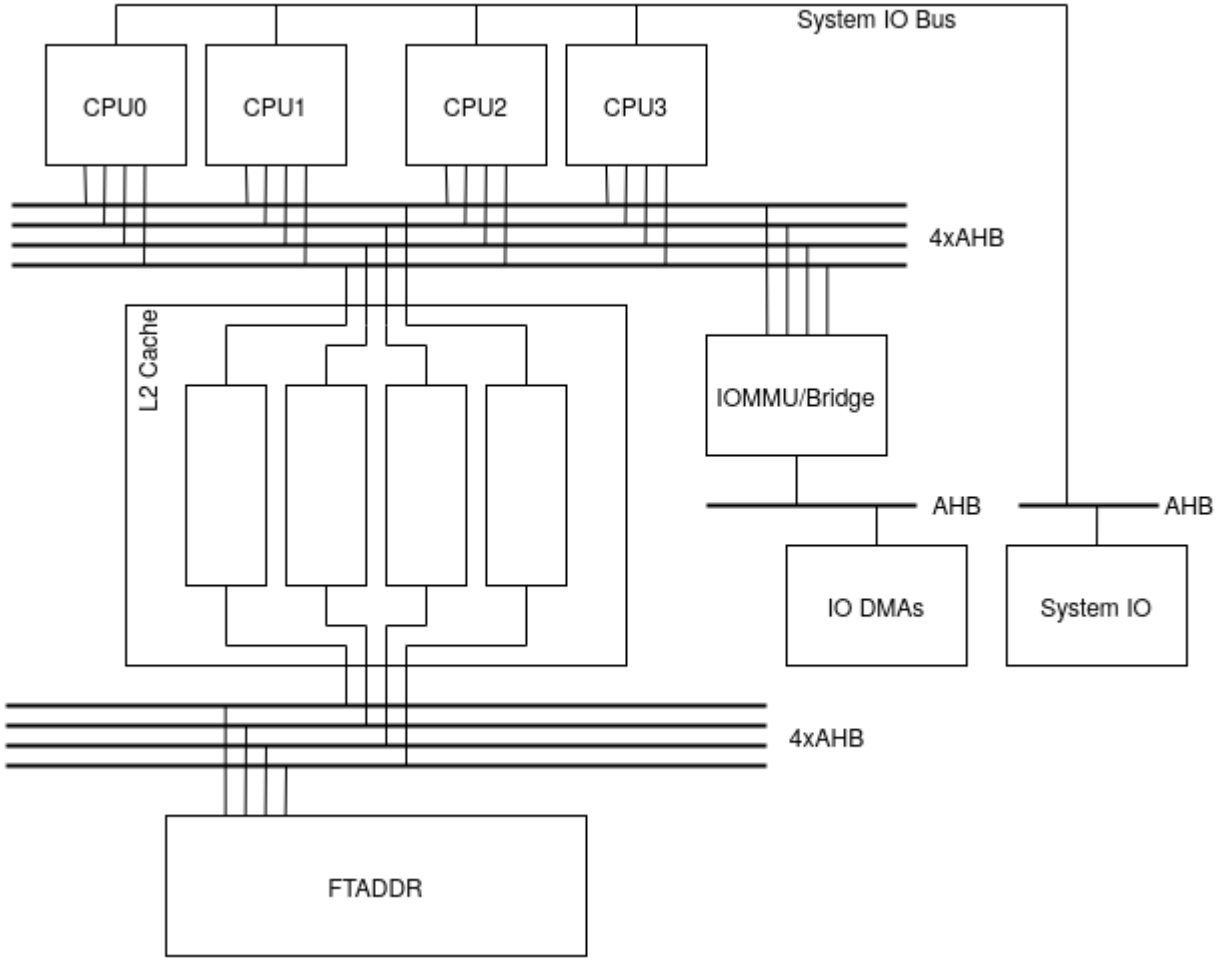
- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC - single component development investment and qualification effort
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.
- De-risking early stages of new application development
  - The architectural choice can be evaluated easily

GR765 – Improved interconnect

- Striped interconnect contains four AHB 2.0 buses
  - All cores connected to all stripes
  - Built in support for larger physical address space, up to 48-bits (GR765 is currently specified to use 36 bits)
- Encoding to stripe based on (configurable) bits in physical address
  - Default setting is to map stripes to cache lines (line 0 stripe 0, next consecutive line would use stripe 1, …)
  - Isolation is achieved by changing the most significant stripe selection bit to a higher logical address bit. Thus, it is possible to separate stripe 0-1 from 2-3.
- Encoding to stripe address space in L1 cache backend
  - Consistent addressing from L1 backend to DDR controller
- Fully isolated L2 cache pipelines dedicated to each stripe.
  - Controlled through a common interface



GR765

The Processor(s)

LEON5 – VHDL IP Overview

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Baseline Features

- **32-bit SPARC V8 processor** core
- **Multi-core support** (AMP & SMP)
- **Improved performance** over LEON3 & LEON4
  - In-order dual-issue Pipeline
- **Improved fault tolerance (FT) from SEUs**
- **Improved FPU**: Floating Point Unit with denormalized number support
- **Leverage existing software:** maintain binary compatibility with LEON3 and LEON4
- **Optional Local RAM** (Tightly coupled memory)
- **Truly portable** between virtually all industry standard technologies and tools
  - ASIC, Xilinx, Microsemi and many more

SPARC Compliant SCD V8

LEON5

https://www.gaisler.com/LEON5

New Fault Tolerant features:
L1 cache SECDED ECC allows error correction on the fly. Optional internal hardware scrubber for L1 and register file

Performance:

- Dhrystone*: 3.23 DMIPS/MHz
  (-O3, inlining allowed)
- Coremark* : 4.52 CoreMark/MHz
  (-O3,-funroll-all-loops -finline-functions -finline-limit=1000)

* All the results generated using BCC 2.0.7 toolchain

NOEL-V Processor Core

RISC-V RV64 and RV32 Processor Model

CAES PIONEERING ADVANCED ELECTRONICS

Characteristics:

- RISC-V 32- and 64-bit compliant processor core
- Superscalar – dual issue
- Fault Tolerance - Error Correction Codes (ECC)
- Leverage foreseen uptake of RISC-V software and tool support in the commercial domain
- Compatible with GRLIB IP Core library
- Highly configurable

Primary feature set:

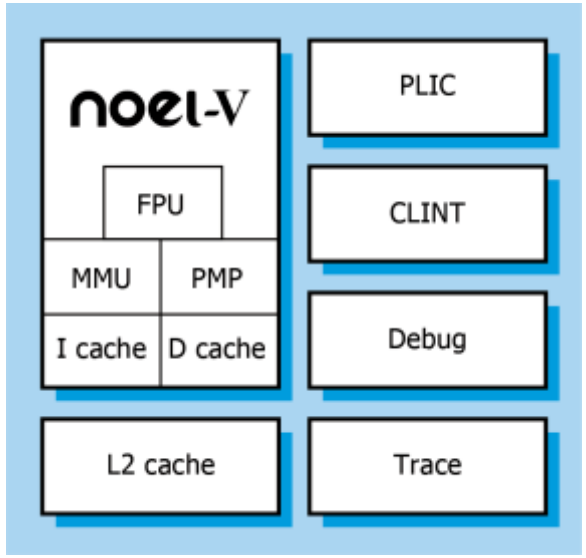
- **RISC-V RV64GCH or RV32GCH**
- AHB and AXI4 bus support

Performance

- Comparable to ARM cortex A53
- CoreMark*/MHz
  - dual-issue 4.41**
  - single-issue 3.05**

https://www.gaisler.com/NOEL-V

noel-V



* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

LEON5 & NOEL-V availability

- LEON5 and NOEL-V are available as part of the GRLIB IP library
  - Dual licensed IP library: GPL variant available at gaisler.com/getgrlib
  - Commercial variants of the library available for different applications (COM, FT-FPGA, FT)
  - The library includes infrastructure for project file generation for most popular EDA tools and SoC template designs
- FPGA bitstreams for Xilinx and Microchip FPGA evaluation boards are available for download (See links below)
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also available

NOEL-ARTYA7

LEON-PF

NOEL-PF

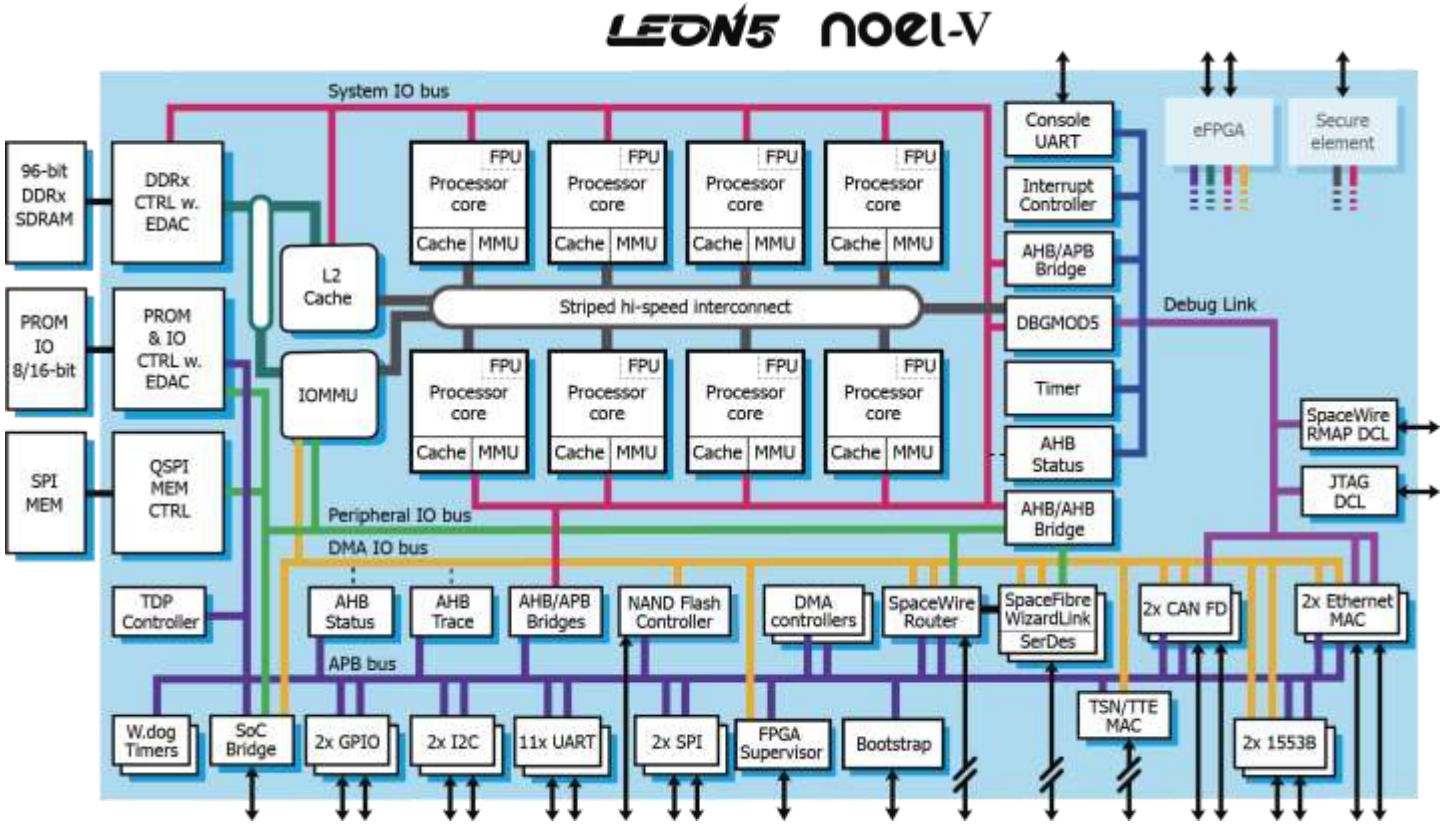
LEON-XCKU

NOEL-XCKU

GR765 – Performance and TSP

Improvements

- Higher computational capacity and improved power consumption.
- **Timing isolation features:** processors can use a subset of the multiple connections to Level-2 cache and memory controller.
- **Improved functional separation features**: secure enclaves and ability to leverage the IOMMU



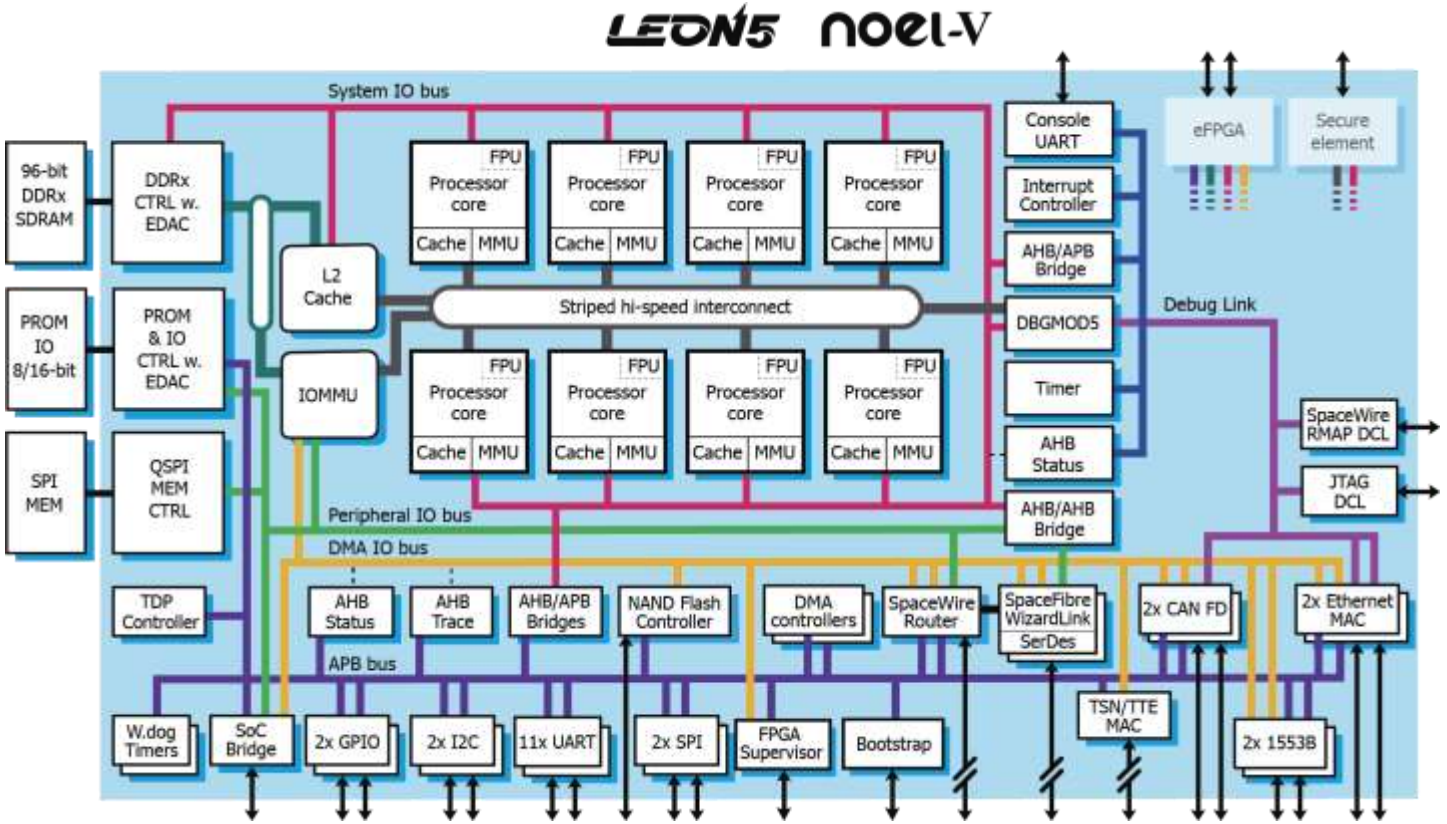
SPARC RISC-V®

GR765 – Functional separation

- **NOEL-V H extension + AIA + IOPMP/MMU**
  - Allows to group IO units together with guest VMs and to separate VMs+IO from each other.
  - Allows for HW distribution of interrupts to guests in hypervisor.

- **Same IOMMU implementation** for both SPARC and RISC-V modes (expected)

- **LEON5FT hypervisor mode** (in development)
- Evaluating use of an additional layer of protection (in addition to processor/IO MMU and PMP) to limit which devices are allowed to access memory-mapped interfaces.
- Additional layer may be necessary in at least LEON5 mode – and will in that case also be available in RISC-V mode.



SPARC RISC-V®

GR765

Interfaces

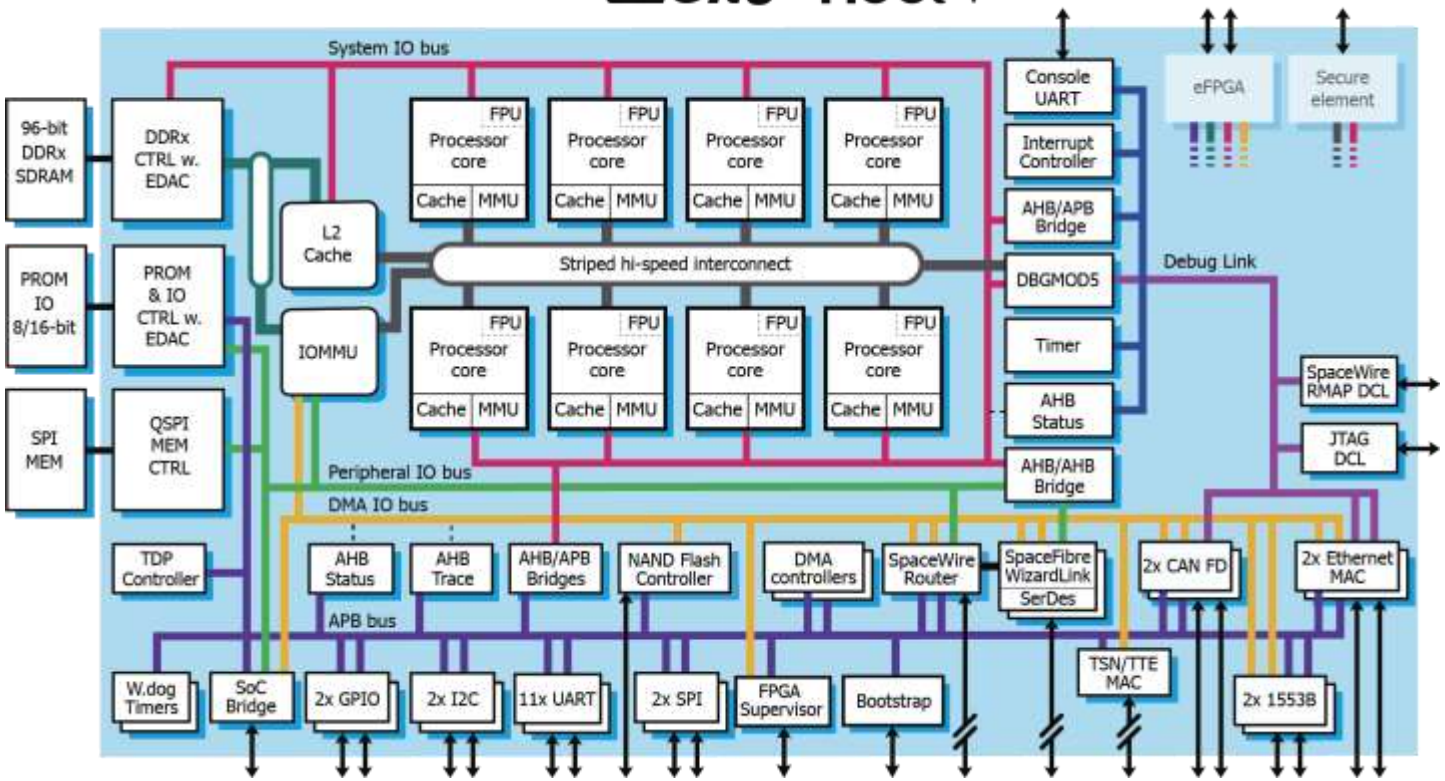
GR765 – Interfaces

Interfaces – SPARC and RISC-V mode

- **SpaceFibre x8 lanes 6.25 Gbit/s, simpler protocols**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet
- **2x or 3x (TBD) TT / TSN Ethernet support**
- **2x** MIL-STD-1553B,
- **2x CAN FD**
- **2x I2C interface**
- **12** x UART
- **2x** SPI controller
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

In development
No guarantee of product launch

LEON5 NOEL-V



SPARC RISC-V®

GR765 – SpaceFibre interfaces

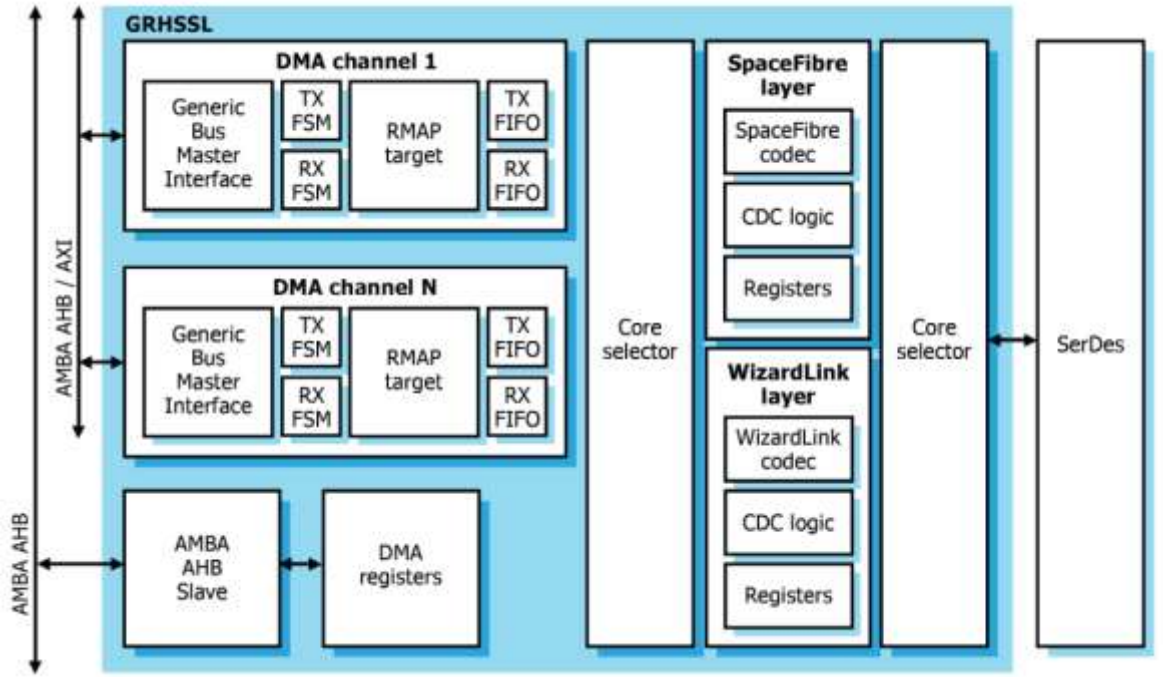
- SpaceFibre codec designed according to the ECSS-E-ST-50-11C standard
- **Flexible DMA engine with multiple DMA channels**: DMA channels operate in parallel and are assigned a subset of Virtual Channels and/or the Broadcast Channel
- **Dedicated RMAP target per DMA channel**: Make use of the dedicated AHB master interface of every channel

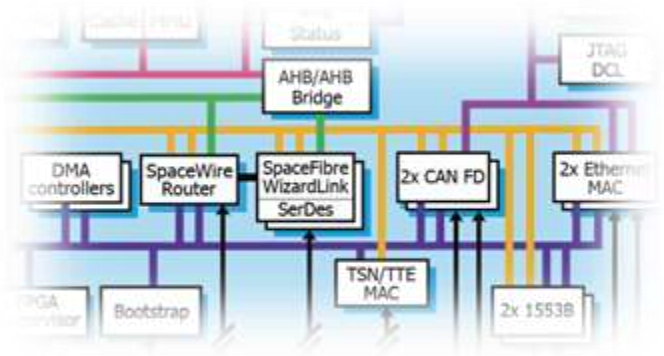
Integration of SpaceFibre with the SpaceWire router

- Bridge between SpaceWire and SpaceFibre traffic. Virtual channels route to SpaceWire router

WizardLink extension

- Companion WizardLink controller designed to interoperate the TLK2711 transceiver. Enable the communication with legacy equipment using custom protocols over WizardLink
- Minimal hardcoded functionality, high degree of configurability



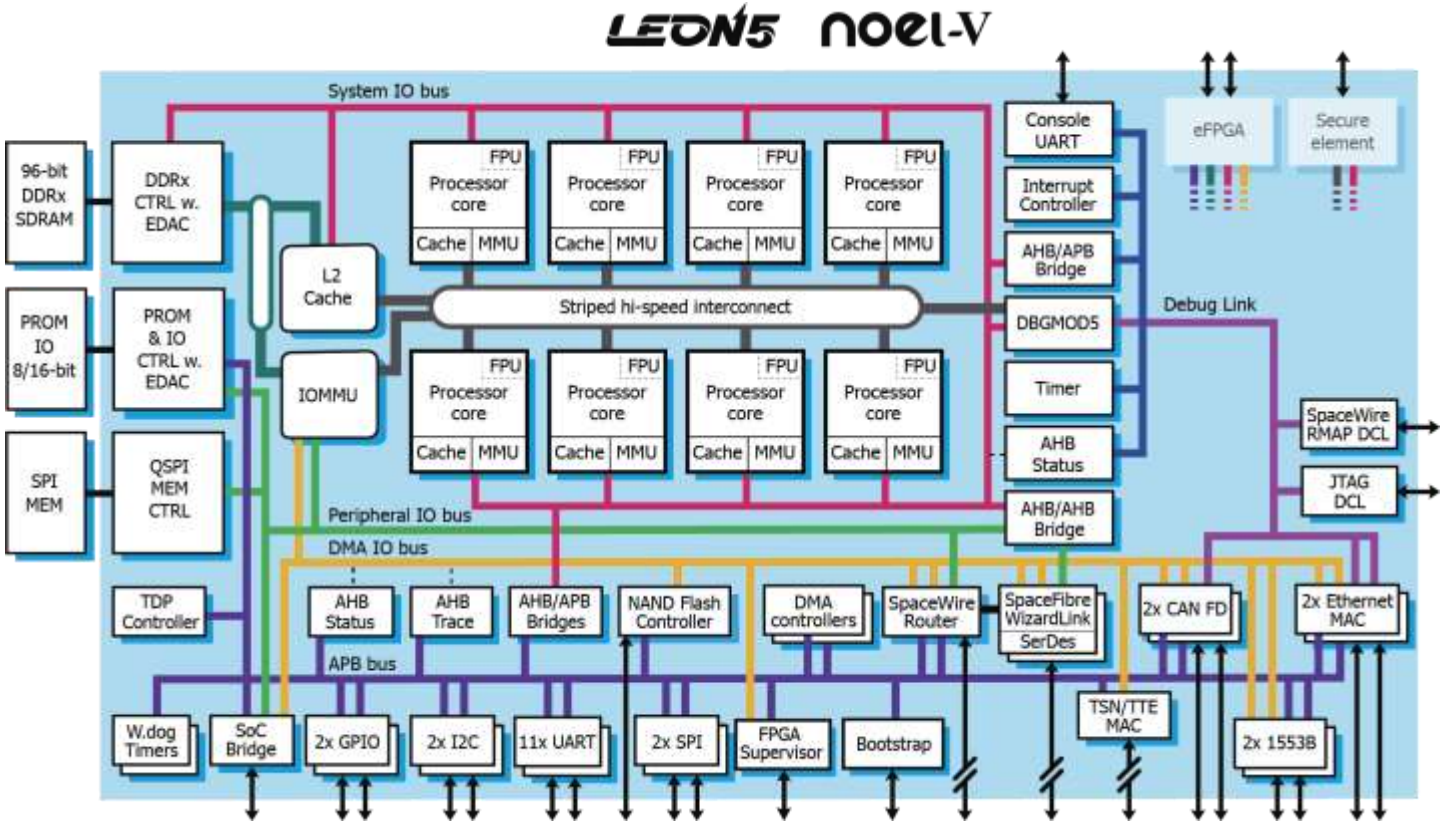


GR765 – Under evaluation

In development
No guarantee of product launch

Under evaluation

- IOMMU extensions – Replace GR740 IOMMU with implementation of RISC-V IOMMU (for both SPARC and RISC-V modes)
- eFPGA fabric vendor selection
- Secure element vendor selection
- NAND Flash NV-DDRx support and support for TLC
- Real-time instruction trace support
  - RISC-V E-Trace encoder implemented
  - evaluating Nexus
- DDR4 support
- PCIe (low probability)



SPARC RISC-V®

Software support

Next-Generation SoC

Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

Tool chains, Operating systems and compilers

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

Hypervisors

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

Boot loaders

- MKPROM2
- GRBOOT Flight bootloader

Tools

- GRMON3
- TSIM3

GR765 and GR740 SW Compatibility

- LEON5FT maintains backward compatibility with LEON4FT.
- Software running on top of environments such as RTEMS, VxWorks, Linux, ... should not require any changes if moving from GR740 to GR765 (updated OS will be provided by CG).
- Example: unmodified LEON3 Linux image will boot on LEON5.
- Redefinition of some internal processor configuration registers, may affect operating system, bootloaders, ….
- Set of communication interfaces is kept and expanded – but PCI is removed
- Changes will be addressed in a **Software Porting Guide**.
  - Versions of communication controller IP may be updated, may require updated software drivers.
  - Memory controllers and pin-mux control are updated.
  - Requires updates to bootloader.
- Significant differences in timing (different processor microarchitecture, memory controller, bus structure, etc).
- Work ongoing to enable same level of software support for NOEL-V as for, and extending beyond, the LEON processors.

LEON5FT and NOEL-VFT 28nm Test Chip on STM FDSOI28 GEO P2

Next-Generation SoC

LEON5 and NOEL-V silicon proven on STM 28nm GEO P2

Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor

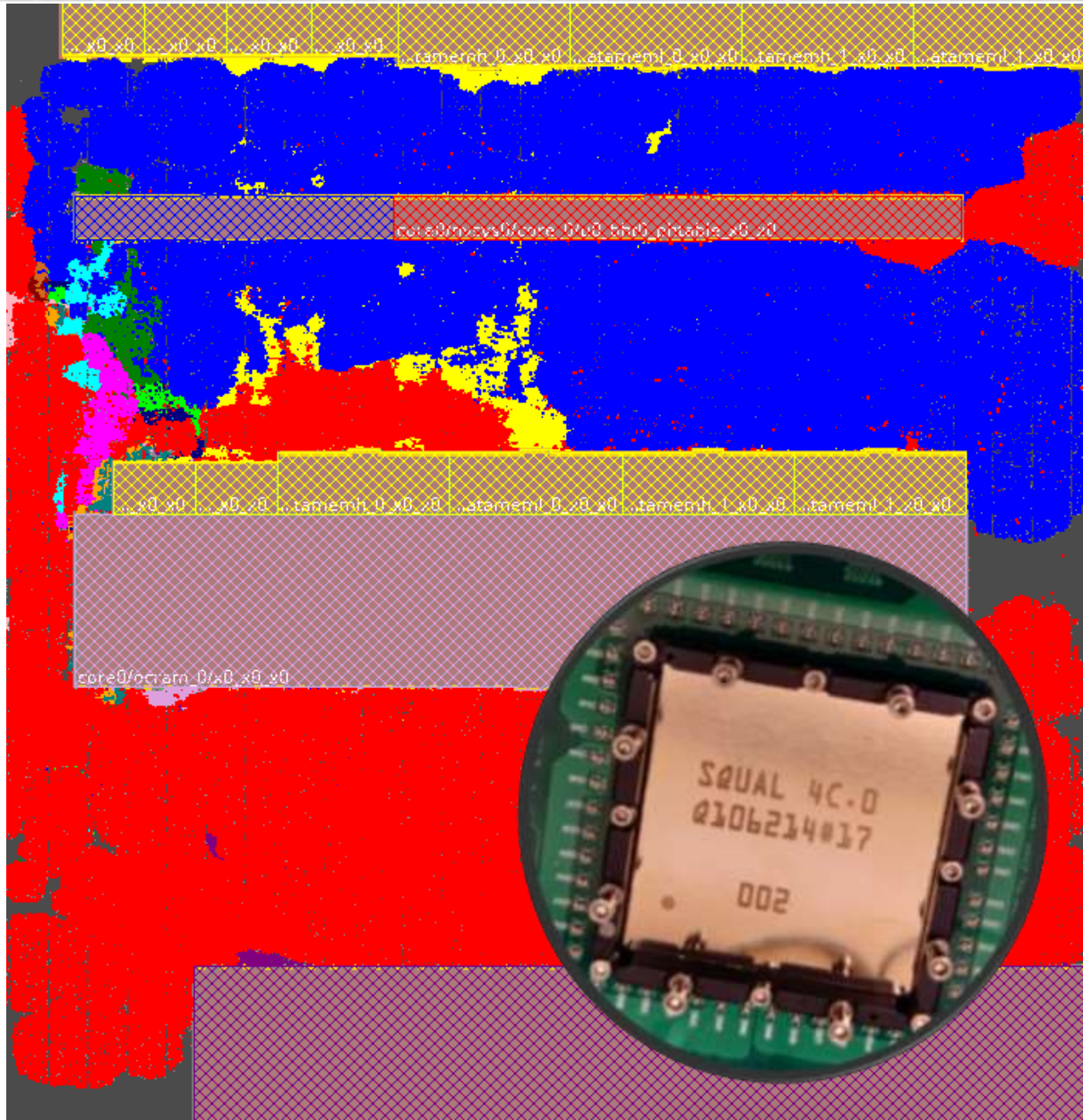
- ST 28nm FDSOI GEO P2 technology
- Specialized design with LEON5 and NOEL-V sharing resources, consumes less than 1 mm^2
- Proves implementation on target technology
- Technology hardness and processor core fault tolerance features demonstrated through SEE test campaign
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain, fab in Crolles (FR)

Performance attained LEON5/NOEL-V:

- Typical corner: 1 GHz / 800* MHz
- Worst-case corner: 600 / 500* MHz

Schedule

- Test chips available at Gaisler
- Performed SEE characterization
- Test chip will be included in GOMX-5 LEO in-orbit experiment



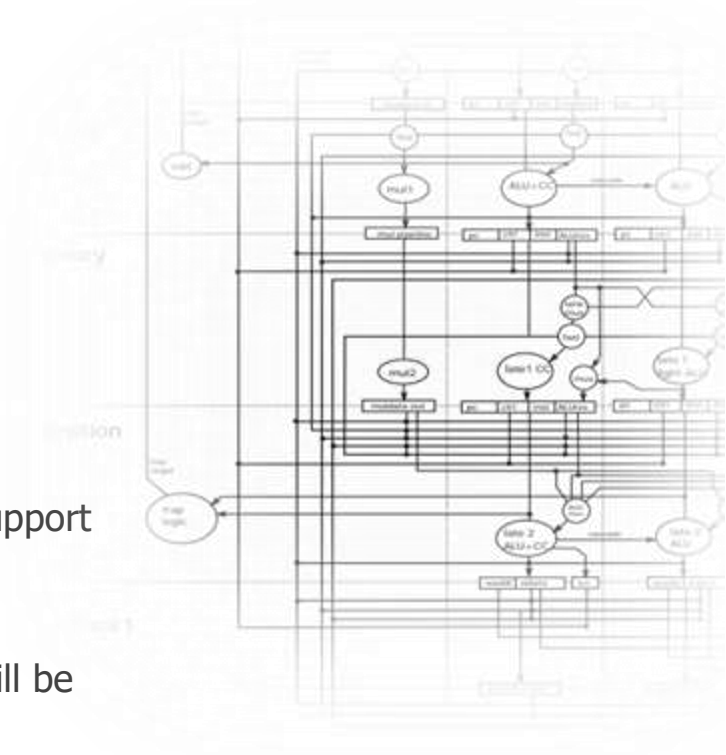
* Following this tape-out, NOEL-V has been further optimized and future implementations are expected to match LEON5 operating frequency.

Conclusion

Next-Generation SoC

GR765 Conclusion

- The GR765 development builds on the successful GR740 quad-core LEON4FT component
- The GR765 is an **octa-core** processor. Users can enable either eight NOEL-VFT RISC-V 64-bit processor cores or eight LEON5FT cores.
- GR765 supports DDR3 SDRAM, high-speed serial link controllers and several other extensions.
- GR765-XX (prototype) components are to be available in 2024.
- The GR765 development puts emphasis on computational performance, power efficiency, and support for mixed criticality application.
- The GR765 is being defined and implemented with focus on the space industry. Feedback can still be addressed, and your input is most welcome.



Progress to be reported via www.gaisler.com/GR765

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