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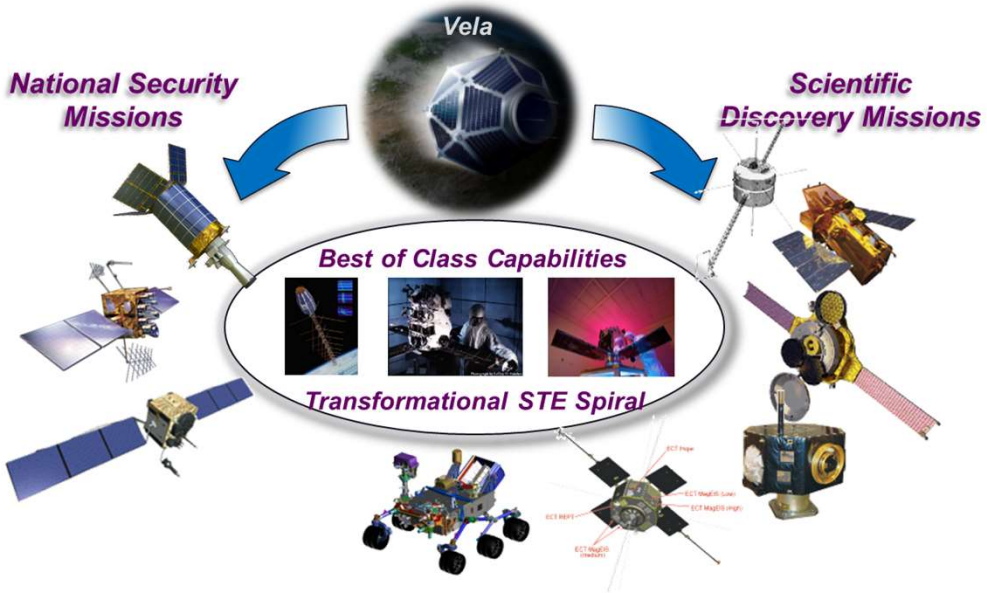
Los Alamos NATIONAL LABORATORY

Hybrid OpenVPX/SpaceVPX Payload Processors using the GR740

Paul S. Graham, Anthony Nelson, Robert Merl, and Justin Tripp

12/15/2022

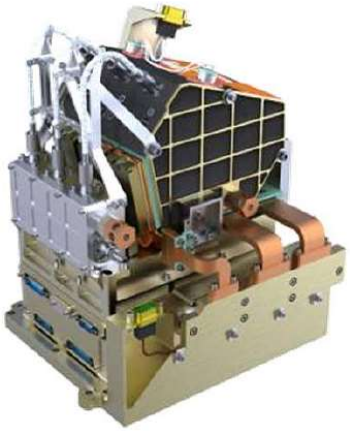
Los Alamos National Laboratory: 50+ Years in Space



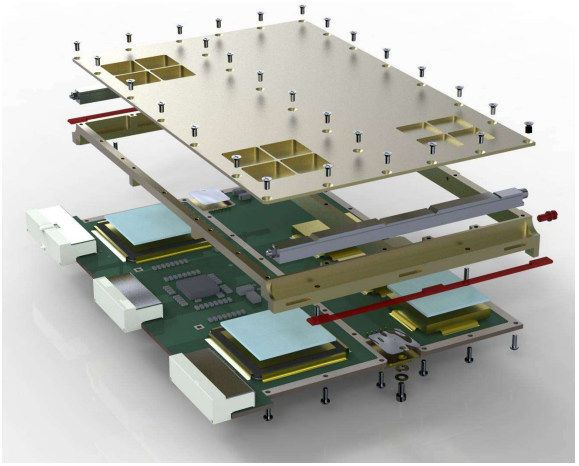
Leveraging Standards for Development and Production

- LANL has benefited from leveraging commercial standards (cPCI, MicroTCA, and VPX) for developing, producing, and deploying systems.
  - For the last 20+ years, LANL shifted from full-custom designs to designs based on commercial standards, resulting in a marked improvement (as much as 2X) in productivity due to
    - design reuse,
    - leveraging commercial infrastructure for development and testing,
    - having more hardware available for parallel development due to reduced production costs and effort, and
    - reduced engineering time.

Full-Custom



Standards -based



Leveraging VPX at LANL

Challenges

- No commercially/widely available SpaceVPX infrastructure for development and testing; many OpenVPX options available
- Differences in control planes for SpaceVPX and OpenVPX (SpaceWire vs. Gb Ethernet)
- SpaceVPX's focus on fully redundant systems: exceeds SWaP constraints for many LANL designs
- OpenVPX lacks fault isolation and recovery mechanisms of SpaceVPX

Approach

- A careful hybridization of OpenVPX and SpaceVPX to
  - Improve the utility of commercial hardware for development,
  - Leverage some fault isolation and recovery mechanisms of SpaceVPX, and
  - Reduce the needed SWaP of the systems.

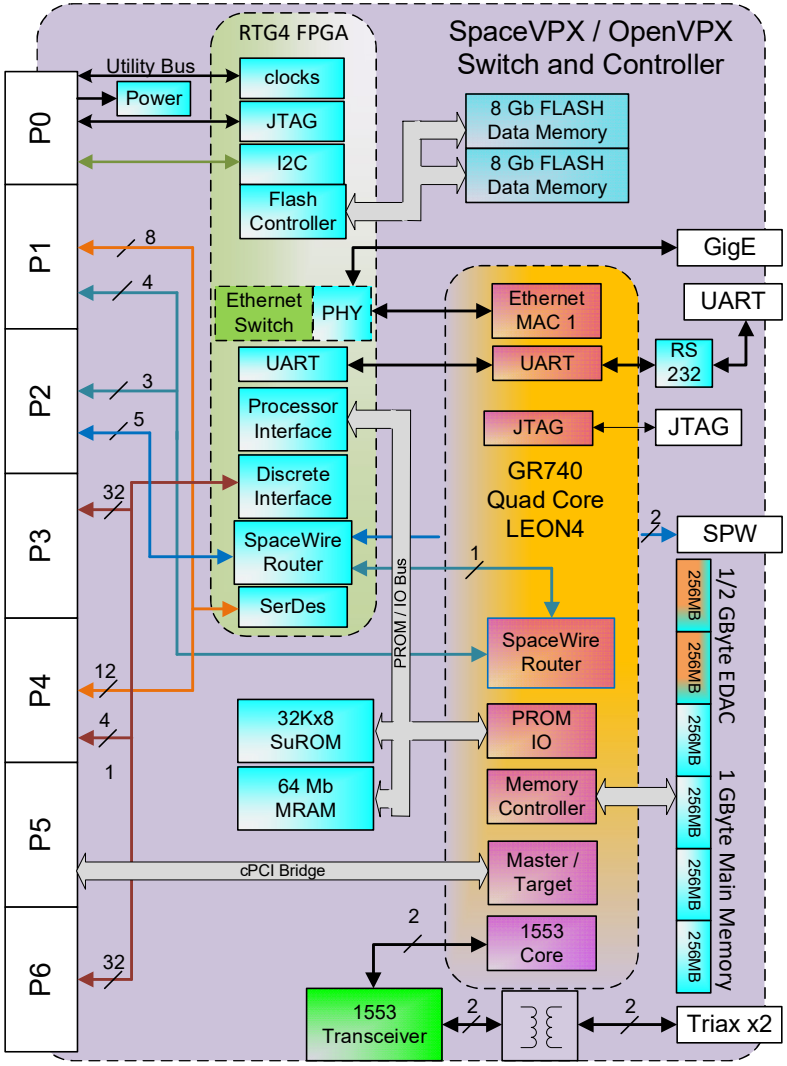
6U Space-Grade Single-Board Computer

- 6U Eurocard VPX
  - 230 mm x 160 mm
  - Interoperable between OpenVPX and SpaceVPX
  - Complies with ANSI/VITA 65.0 and 78.0
    - Hybridization of SLT6-SWH-16U20F-10.4.2 (VITA 65.0-2021) and SLT6-SWC-16T12F12U-10.4.1(VITA 78.0-2022) System Controller and Switch slot profiles
- Design Goals for use in GEO / MEO / LEO Orbits
  - 100-krad TID
  - Latch-up immunity: 103 MeV/mg/cm^2
  - Mechanically Hardened
  - Meets or exceeds NASA GEVS for shock, vibration, thermal
  - Conduction-cooled Frame
  - Hypertac Connectors
  - QML-V or Class S components
- Low Power / 8.5 W
- Design licensed to CAES

Image of first revision of the 6U OpenVPX/SpaceVPX processor board

Initial 6U Design

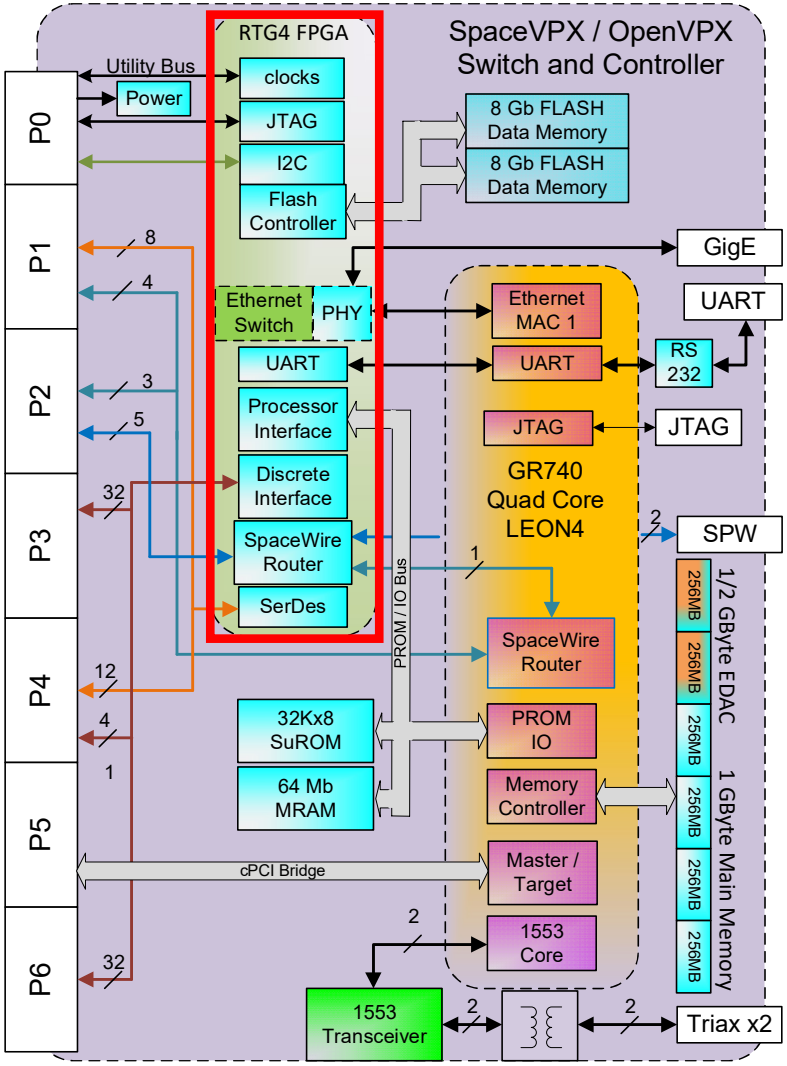
- CAES Quad-Core LEON4 GR740 Processor
  - GFLOP performance @ 250 MHz
  - 1 GiB SDRAM / 0.5 Gbyte EDAC
  - 2 GiB Non-Volatile Storage
  - PROM / Flash / SDRAM memory hierarchy
- VxWorks and RTEMS RT Operating Systems
- Common Space-Grade Interfaces
  - SpaceWire
  - I2C
  - Discrete I/O (single-ended and differential)
  - MIL-STD-1553B
  - UARTs
  - Multi-gigabit serial transceivers
  - PCI
- Reconfigurable Microchip RTG4 FPGA



Block diagram of the 6U OpenVPX/SpaceVPX processor card

Flexible and Reconfigurable Interfaces

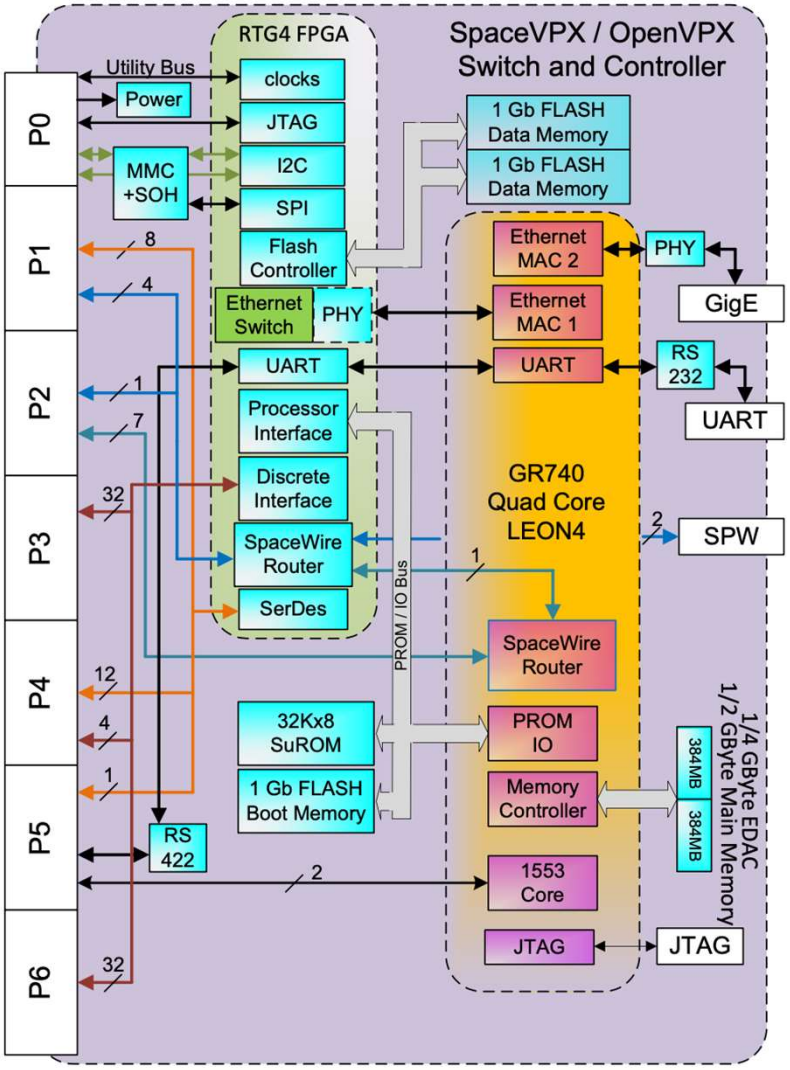
- Reconfigurable Microchip RTG4 FPGA
  - Provides a method for extending the I/O standards and peripherals supported by the single-board computer (SBC)
    - I2C, JTAG, multigigabit serial transceiver protocols (Gb Ethernet, Serial Rapid IO, etc.)
    - Additional memory interfaces, overcoming limitations of PROM/IO Bus
  - Makes I/O configurable for each application
    - FPGA LVDS and single-ended I/O can be programmed by application need
    - Add protocol-specific switches in FPGA fabric, as needed (SpaceWire, Ethernet, etc.)



Block diagram of the 6U OpenVPX/SpaceVPX processor card

Revised 6U Design

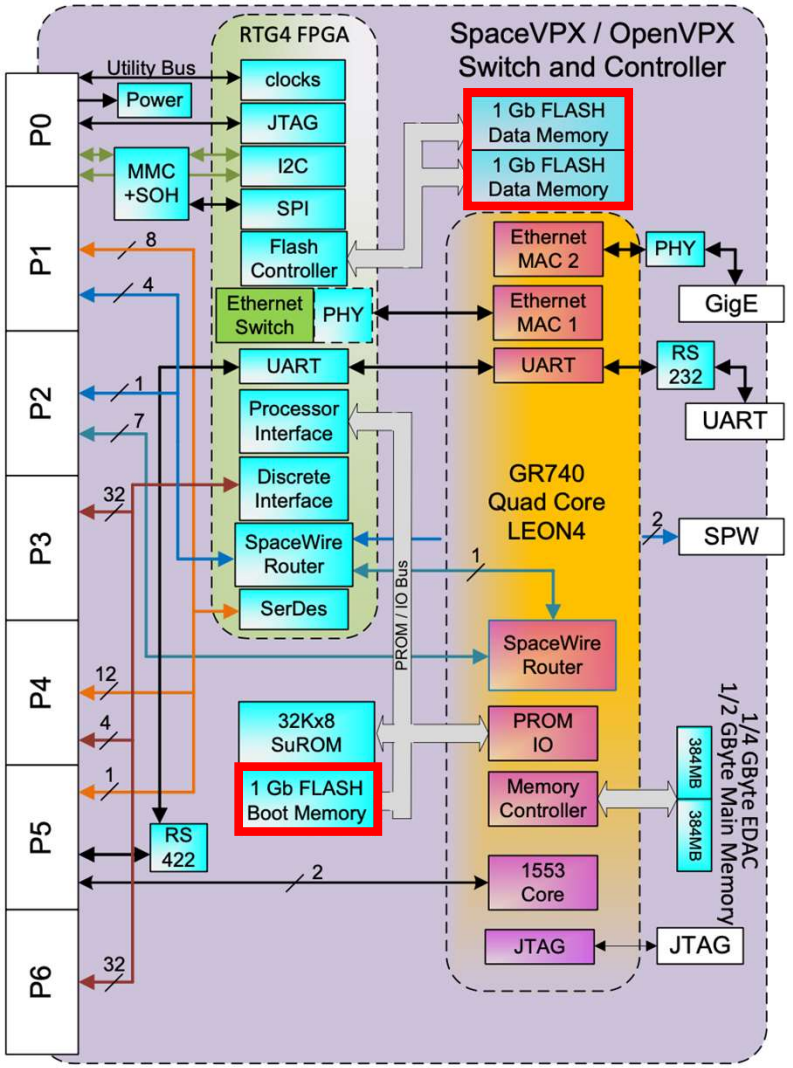
- Changes driven by internal customer needs and opportunities for improvement in first design
  - PCI no longer needed
  - 1553 XCVR and magnetics on separate board
  - Added RS-422 XCVR for UART
  - Microcontroller for state-of-health measurement and chassis management controller (optionally)
  - Memory and feature trade-offs (see upcoming slides)
    - 512 MiB of SDRAM / 256 MiB of EDAC
    - 384 MiB of Non-Volatile Storage
    - Additional Ethernet interface for development with rad-tolerant PHY



Block diagram of the Revised 6U OpenVPX/SpaceVPX processor card

Design Trade-Offs: Non-volatile Storage Density vs. Hardness

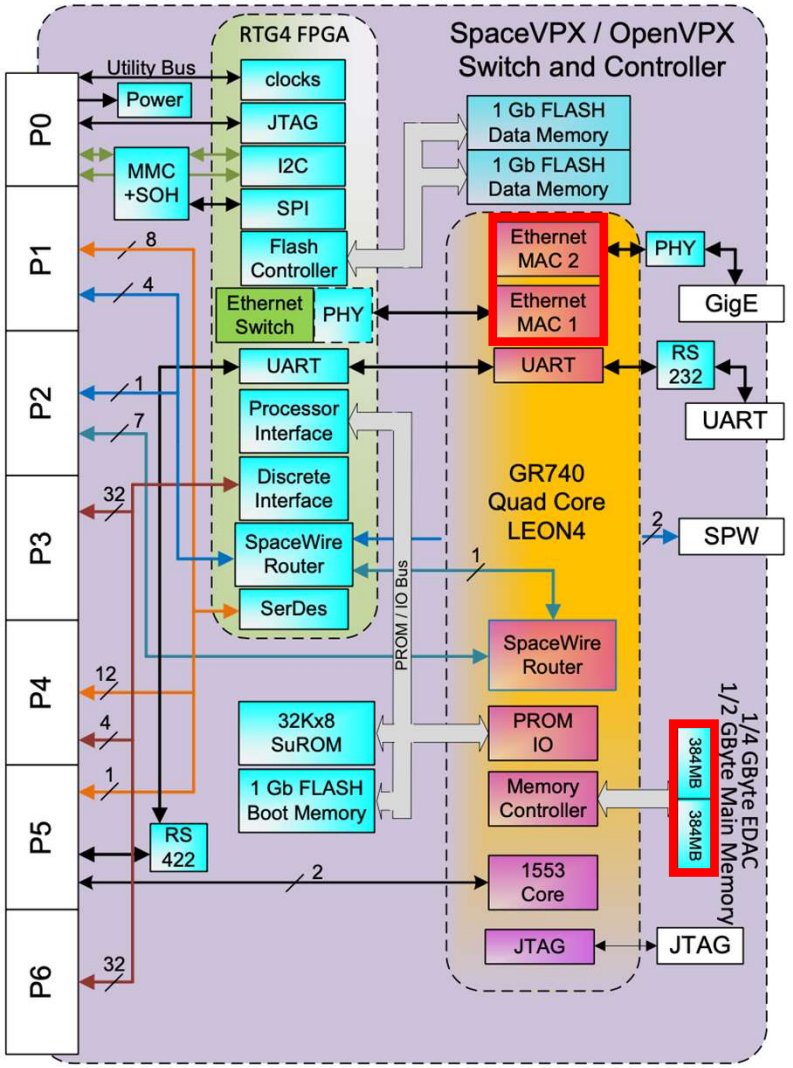
- The original design had 2 GiB of NAND flash, but those memories were limited to 70-krad TID even after extra screening.
- Internal customers prioritized radiation hardness over storage density for the non-volatile memory, so we chose to use CAES 128-MiB, 300-krad TID NOR flash for the revised design, for a total of 384 MiB of storage.
  - 256 MiB of data storage (behind the RTG4 due to limited chip selects on the PROM/IO bus)
  - 128 MiB of boot storage (replacing an 8-MiB MRAM)



Block diagram of the 6U OpenVPX/SpaceVPX processor card

Design Trade-Offs: SDRAM Density, SDRAM Bandwidth, Ethernet Connectivity

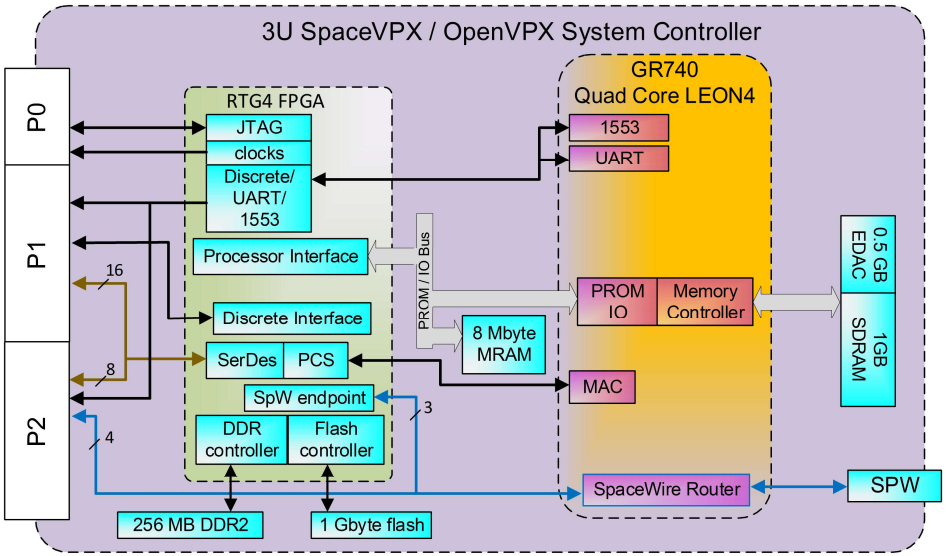
- SDRAM components used in the original design had excessive loading on some chip selects due to packaging design, limiting memory performance.
- Evaluated revised memory architectures using alternative components
  - Option 1: 96-bit-wide memory interface
    - Not available in original design due to pin-sharing with PCI
    - Maximum memory bandwidth and density: 96-bit-wide interface with 1 GiB of ECC-protected SDRAM running at 50 MHz (est.)
    - Single Ethernet port available due to pin-sharing with 2nd Ethernet interface and upper 48-bits of SDRAM interface
  - Option 2: 48-bit-wide memory interface
    - Reduced memory density and bandwidth: 48-bit-wide interface with 512 MiB of ECC-protected SDRAM running at 70-80 MHz (est.), ½ the RAM at 70-80% of the bandwidth
    - Two Ethernet ports: one for front panel (development) and another to the FPGA for high-speed interface or ***future support*** of SERDES-based Ethernet (1000BASE-KX/BX and possibly an Ethernet switch)
- Went with Option 2, which met the current SDRAM needs while providing improved connectivity



Block diagram of the 6U OpenVPX/SpaceVPX processor card

3U Design

- Based on original 6U design
- Quad Core LEON4 / GR740 Processor
  - GFLOP performance at 250-MHz core clock
  - 1 GiB SDRAM / 0.5 GiB EDAC
  - MRAM / SDRAM memory hierarchy (No ROM)
  - 1 GiB of flash (instead of 2 GiB)
- VxWorks and RTEMS RT Operating Systems
- Common Space-Grade Interfaces
  - SpaceWire
  - I2C
  - Discrete IO
  - UART
  - MIL-STD-1553B (external magnetics required)
  - 12 lanes of Ethernet / high speed serial at up to 3.125 Gb/s
- Reconfigurable RTG4 FPGA
  - DDR2 SDRAM to support FPGA co-processing
  - Potential JESD204B support for direct connection to digitizer / instrument cards



3U Single-Board Computer
Block Diagram and Image

Additional Comments

- Highest bandwidth interfaces between the GR740 and the FPGA are SpaceWire and Ethernet
  - PROM/IO interface for low-bandwidth control
  - Different from previous designs based on GR712 where FPGA sat on wider, faster, deeper memory interface
- Having an FPGA as a companion to the GR740 provides
  - a lot of flexibility in supporting different applications with a single hardware design, especially, those with differing I/O needs;
  - an interface that can be used to connect to high-speed networks with SERDES interfaces (with some firmware development); and
  - a method to add more network switching capabilities to the SBC (with some firmware development).
- The GR740 has proven to be a reliable and productive basis for our SBCs.